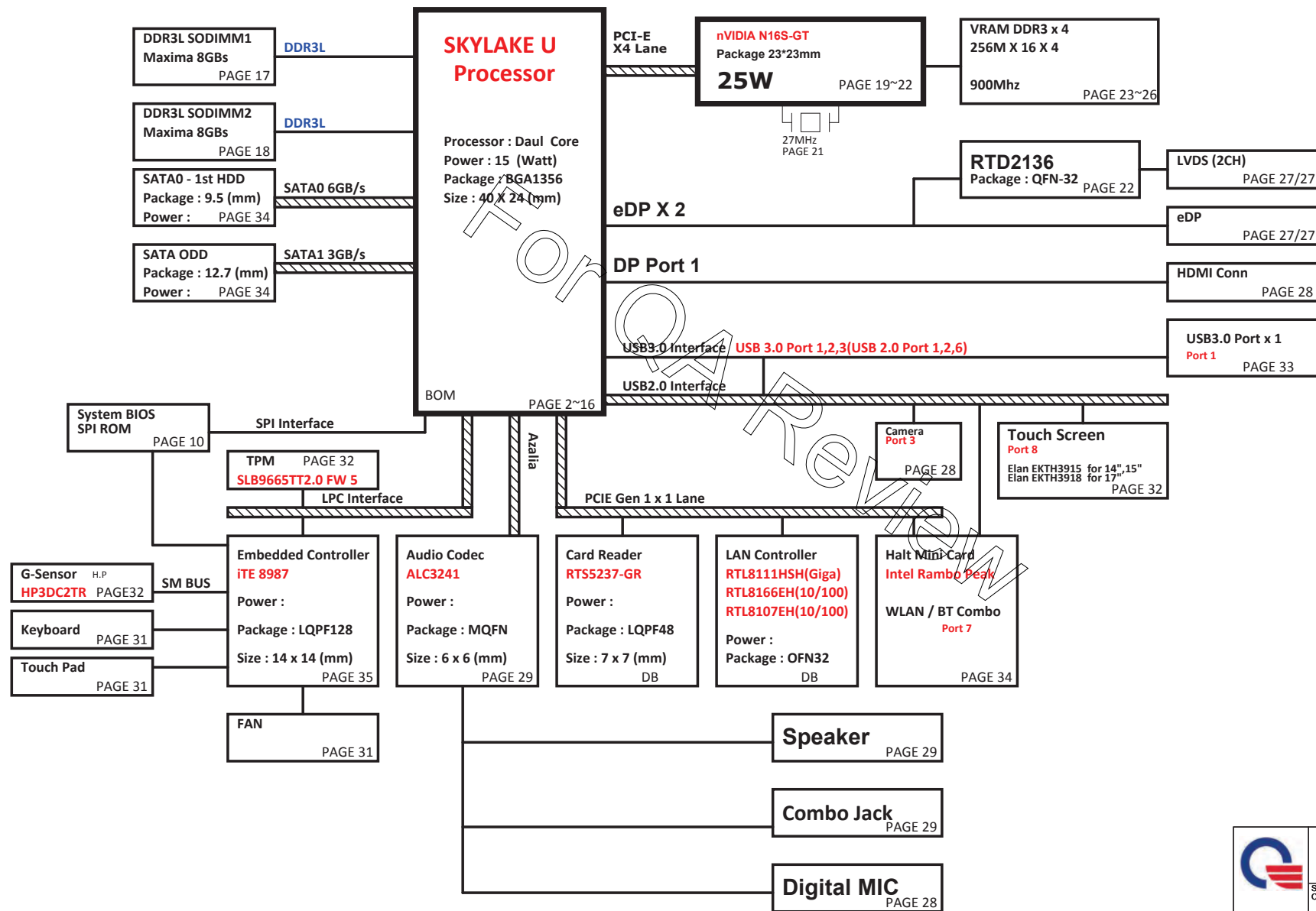


# DIS (14" / 15" / 17") Chocolate Intel SKYLAKE ULT Platform Block Diagram

PCB 6L STACK UP

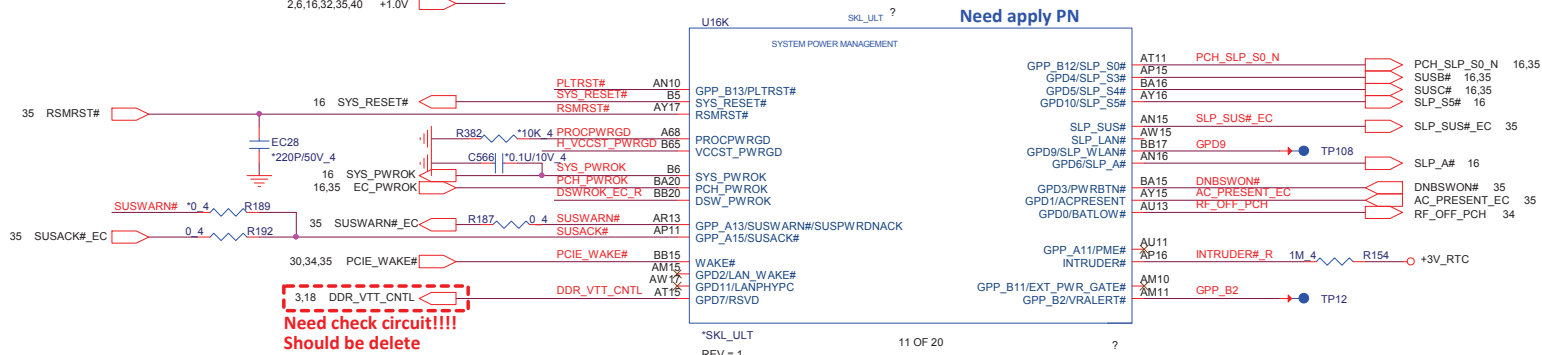
LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1(High)  
LAYER 4 : IN2(Low)  
LAYER 5 : SVCC  
LAYER 6 : BOT



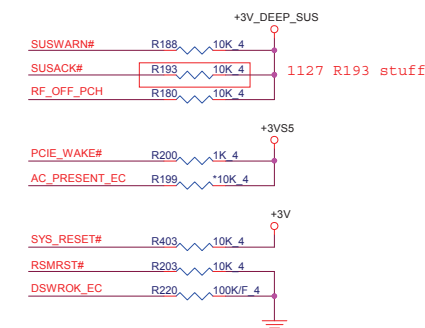




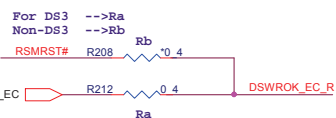
10,11,12,14,15,16,18 +3V\_DEEP\_SUS  
2,10,11,12,13,14,15,16,17,18,20,27,28,29,30,31,32,33,34,35,41,43,44 +3V  
10,15,16,32,34,35,37,39,40,43,46 +3VS5  
2,5,6,9,40,41 +VCCSTPLL  
2,6,16,32,35,40 +1.0V



## PCH Pull-high/low(CLG)



## For DS3 Sequence

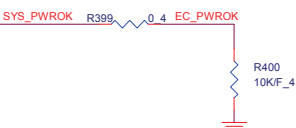
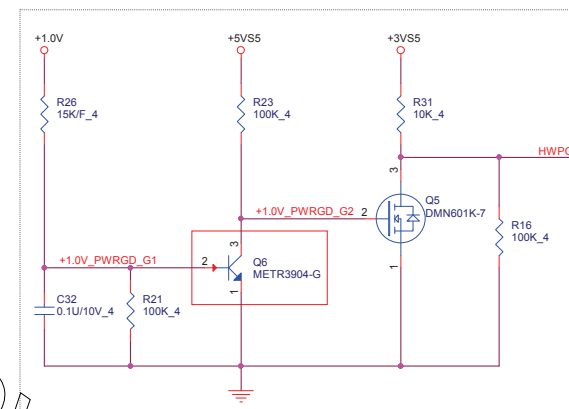
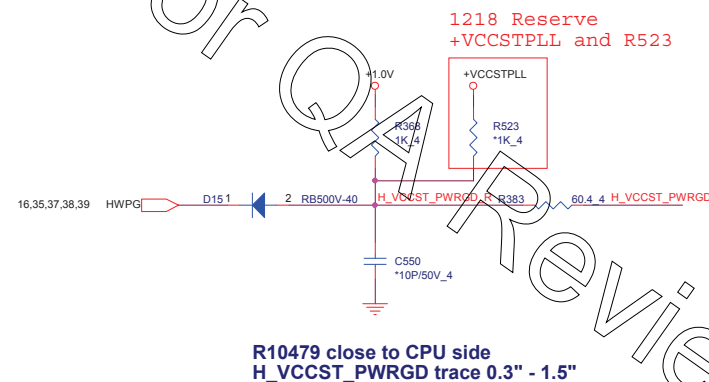


## PLTRST#(CLG)

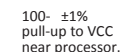
Check Q2010 Rise/Fall time less than 100ns



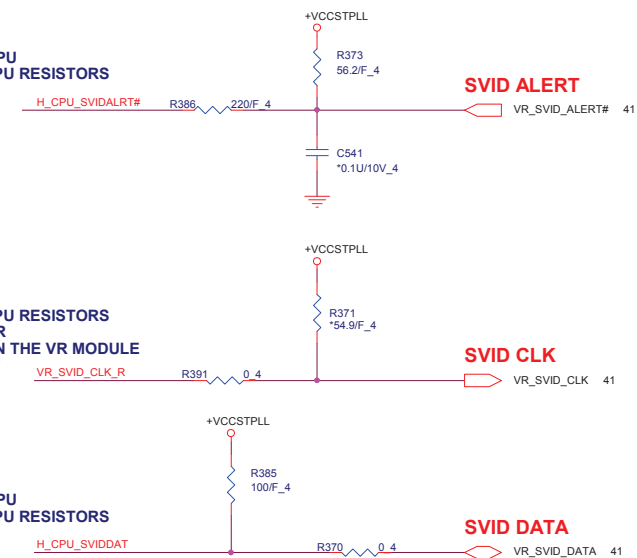
## System PWR\_OK(CLG)

1218 Reserve  
+VCCSTPLL and R523

		<b>PROJECT :Y11X-6L</b>	
		Quanta Computer Inc.	
Size Custom	Document Number <b>04 - SKYPAKE 5/20(Power Manger)</b>	Rev 1A	
Date: Wednesday, May 06, 2015	Sheet	4 of	49




**CLOSE TO CPU  
PLACE THE PU RESISTORS**



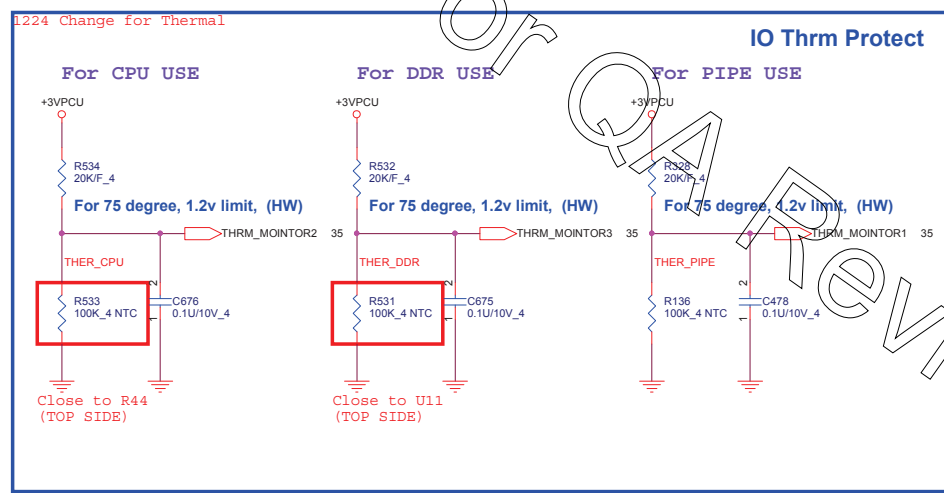
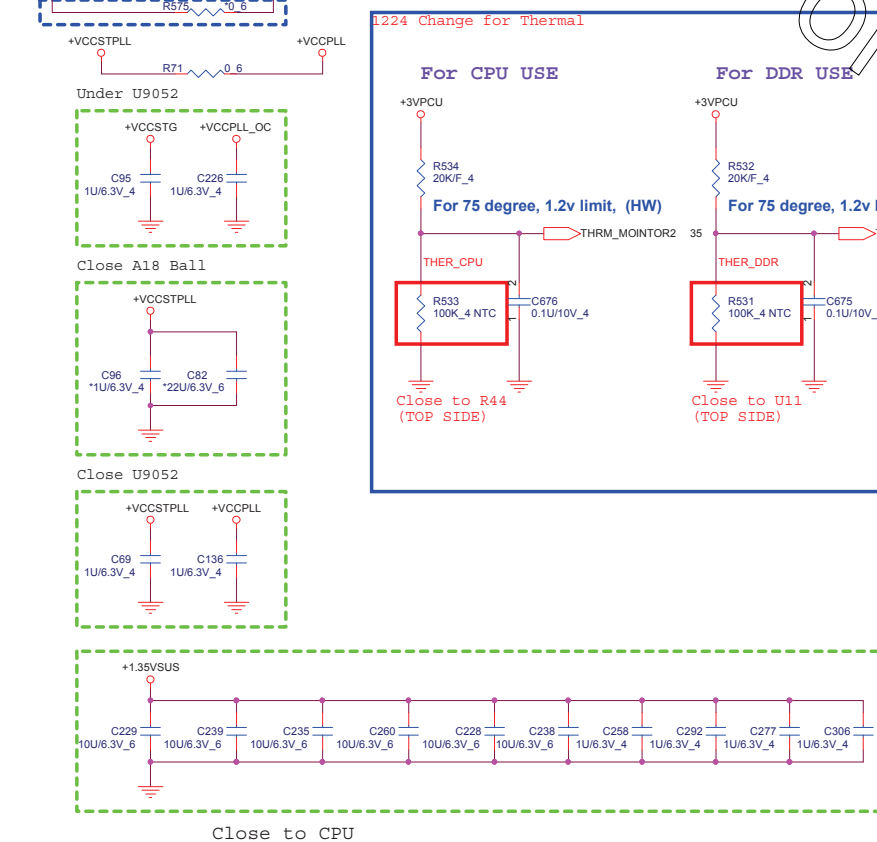
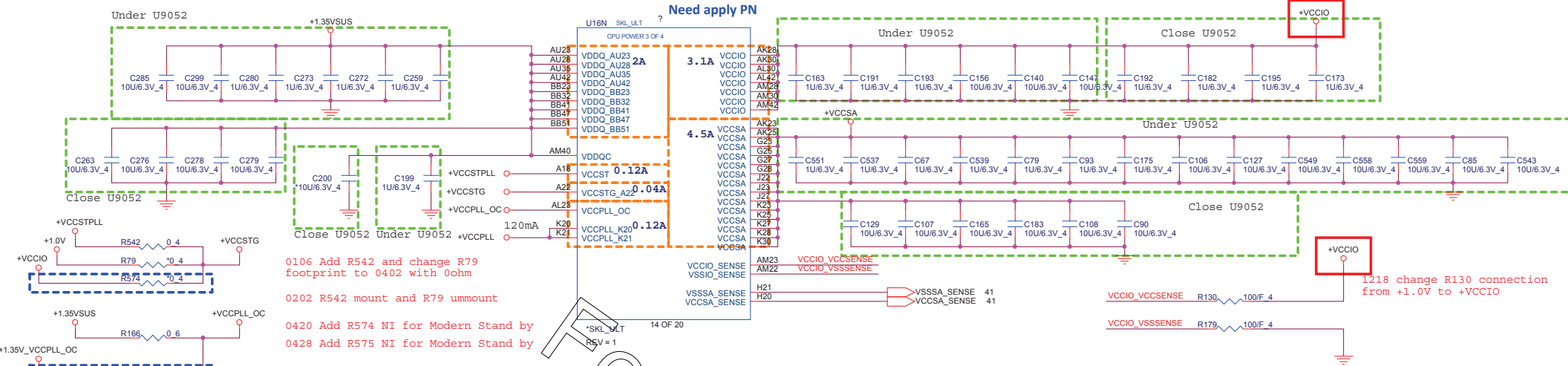
PLACE THE PU RESISTORS  
CLOSE TO VR  
PULL UP IS IN THE VR MODULE

**CLOSE TO CPU  
PLACE THE PU RESISTORS**

	<b>PROJECT :Y11X-6L</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number <b>05 -- SKYPAKE 6/20 (POWER-1)</b>	Rev 1A
	Date: Wednesday, May 06, 2015	Sheet	5 of 49



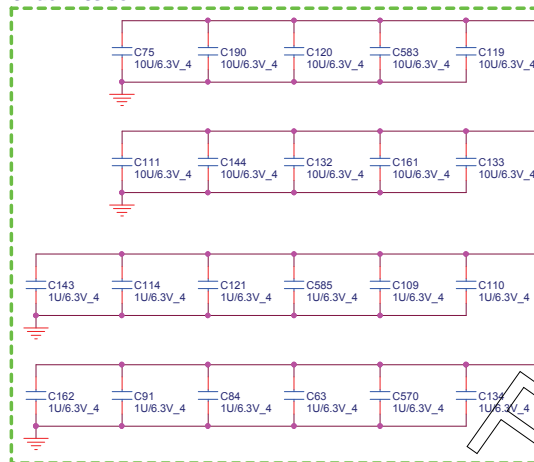
Input	Pin Numbers
+VCCSTPLL	2,4,5,9,40,41
+VCCSA	41,42
+1.35VSUS	3,17,18,38,40,46
+1.0V_DEEP_SUS	9,13,15,16,39,40
-1.0V	2,4,16,32,35,40
+3VPCU	13,30,31,32,33,34,35,36,37



Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
V <sub>CCGTx</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCIO</sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_VFS</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCEOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

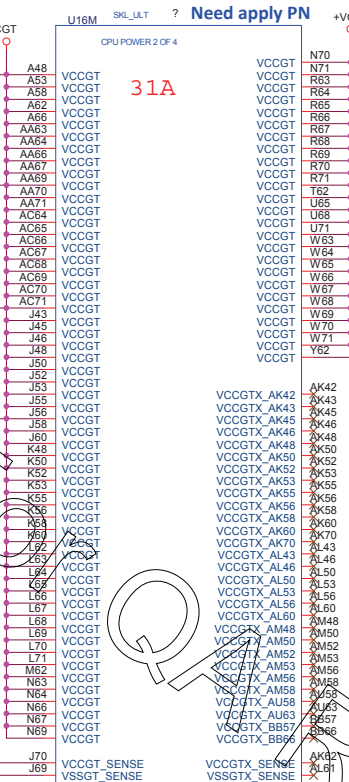
+VCCGT 41  
+VCC\_CORE 5,41  
+1.35VSUS 3,6,17,18,38,40,46

Under U9052



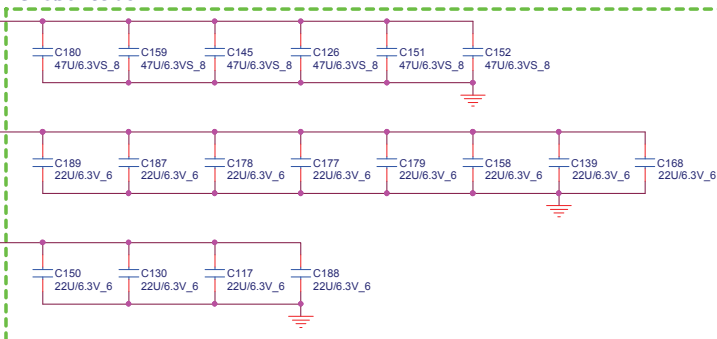
U16M SKL\_ULT ? Need apply PN

31A



+VCCGT

Close U9052




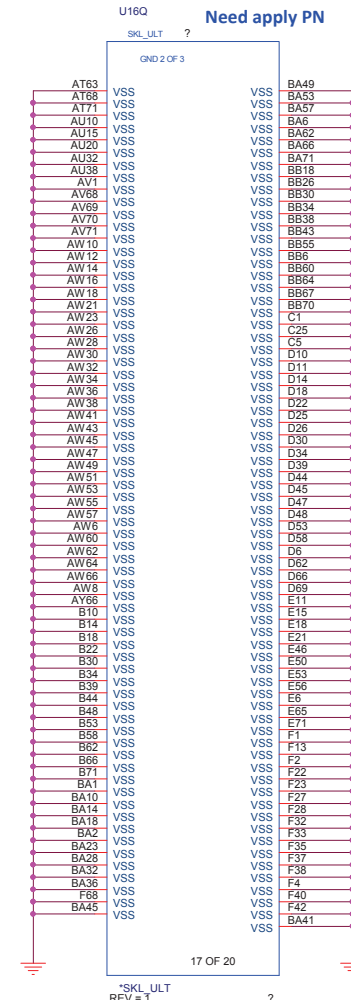
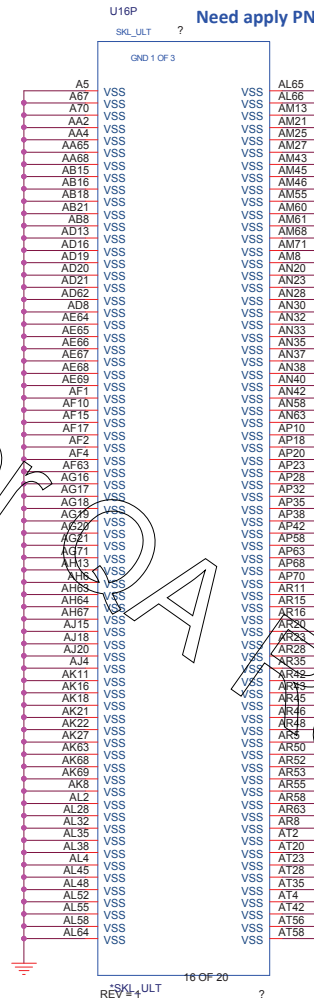
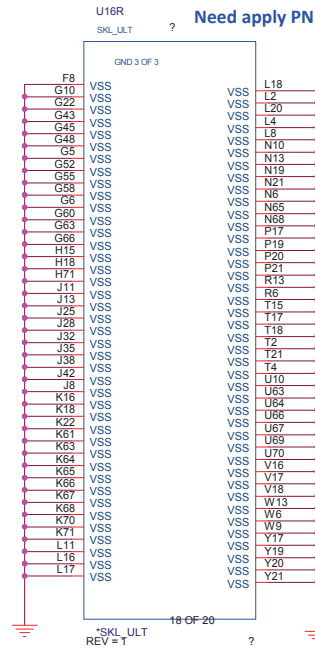
41 VCCGT\_SENSE  
41 VSSGT\_SENSE

J70 VCCGT\_SENSE  
J69 VSSGT\_SENSE

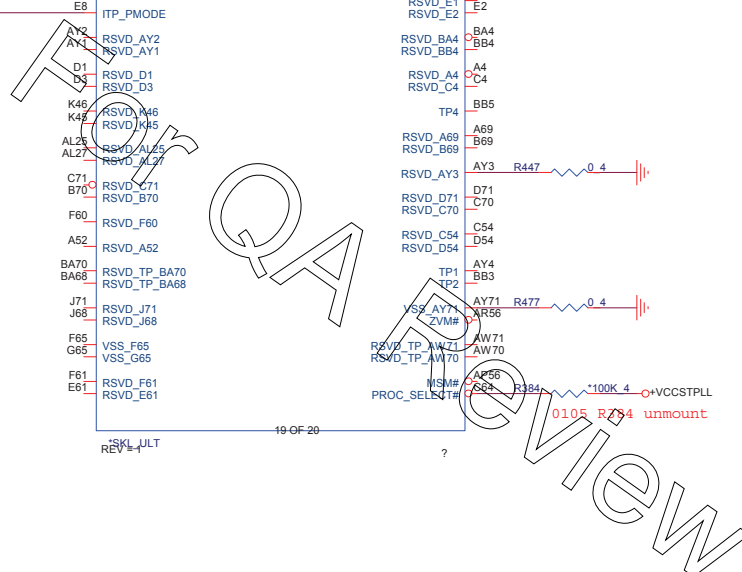
\*SKL\_ULT 13 OF 20  
REV = 1

Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
V <sub>CCGTX</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCIO</sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_LPB</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCEOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

 <b>PROJECT :Y11X-6L</b> Quanta Computer Inc.		
Size Custom	Document Number <b>07 - SKYPAKE 8/20 (POWER-3)</b>	Rev 1A
Date: Wednesday, May 06, 2015	Sheet	7 of 49







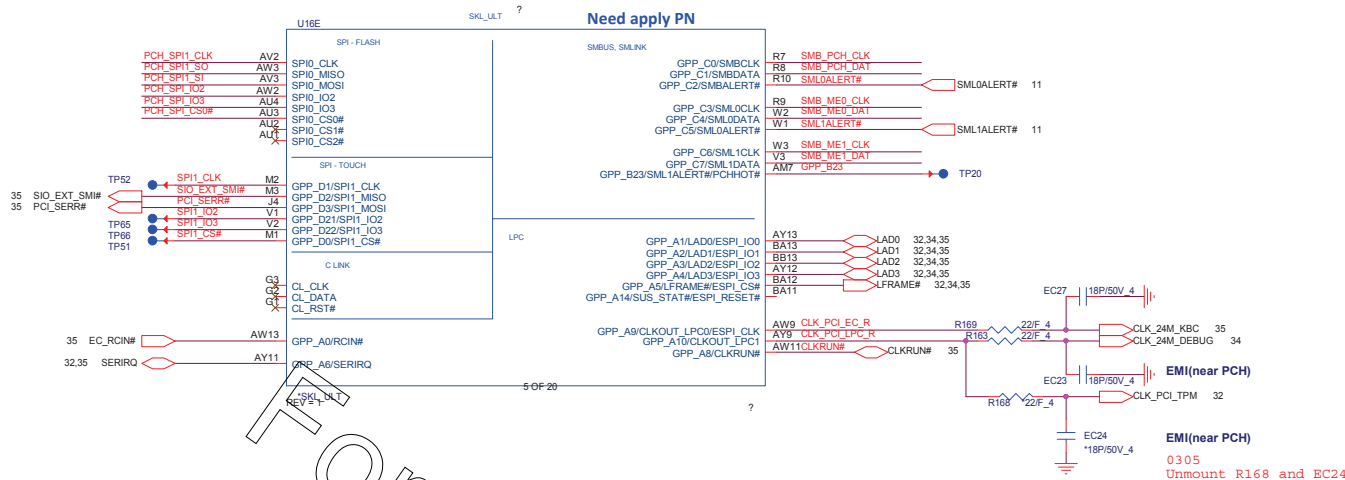
CFG3 (Physical Debug Enable) DFX Privacy
CFG4 (DP Presence Strap)

1

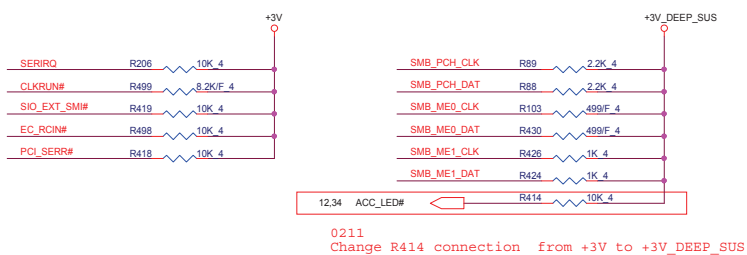
---

No physical DP attached to eDP

1
Disable:
Disable; No physical DP attached to eDP

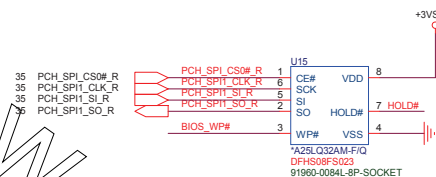


## PCH SPI ROM (CLG)



Vendor	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

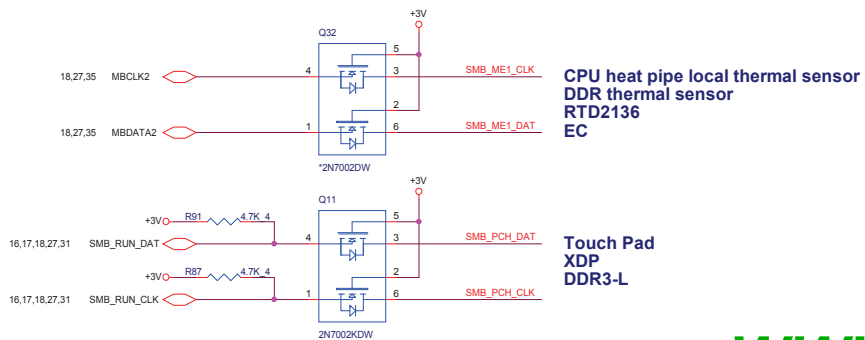
### 4M SPI ROM Socket



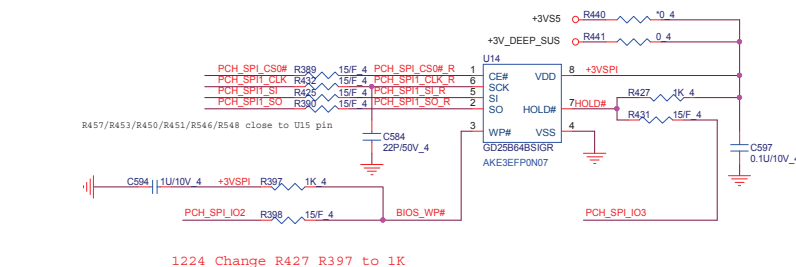
```
0211
Change mount U14, unmount U15
```


U23&U24 footprint 要重疊

### SMBus/Pull-up(CLG)



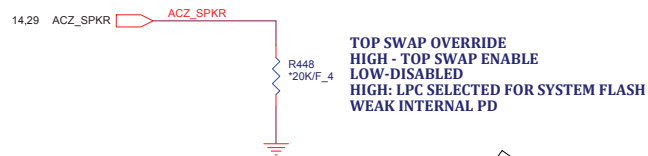
## PCH SPI ROM(CLG)



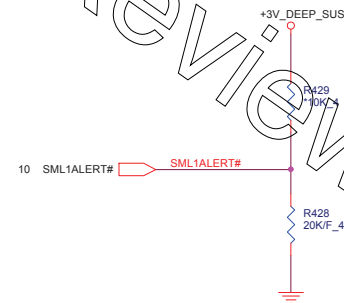
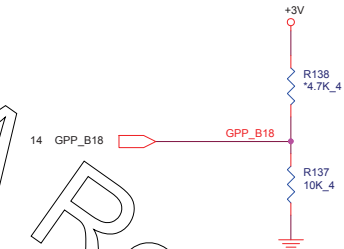
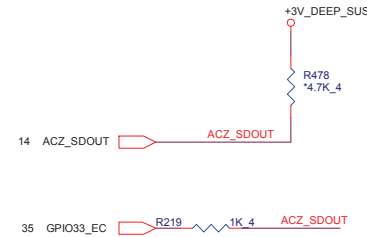
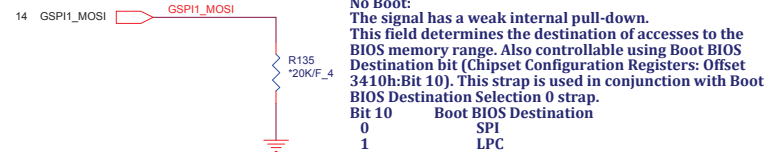
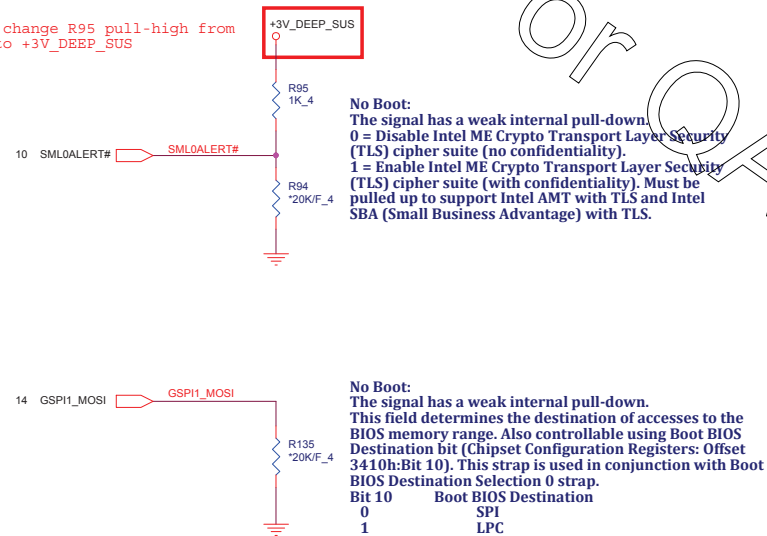
	<b>PROJECT :Y11X-6L</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number <b>10 -- SKYPAKE 14/20(SPI/LPC/SMBUS)</b>	Re 1
Date: Wednesday, May 06, 2015		Sheet 10of 49	


# Functional Strap Definitions

**DESIGN NOTE:**  
WEAK PULL UP RESISTOR PRESENT ON THIS NET



1212 change R95 pull-high from +3V to +3V\_DEEP\_SUS



 <b>PROJECT :Y11X-6L</b> Quanta Computer Inc.		
Size Custom	Document Number <b>11 - SKYPAKE 15/20(HDA)</b>	Rev 1A
Date: Wednesday, May 06, 2015	Sheet	11 of 49

+3V 2,4,10,11,13,14,15,16,17,18,20,27,28,29,30,31,32,33,34,35,41,43,44  
 +3V5S 4,10,15,16,32,34,35,37,39,40,43,46  
 +3V\_DEEP\_SUS 4,10,11,14,15,16,18



PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	dGPU	Port0	Un-used
Port2	dGPU	Port1	CardReader
Port3	dGPU	Port2	WLAN
Port4	dGPU	Port3	LAN
Port5	CardReader	Port4	VGA
Port6	WLAN	Port5	Un-used
Port7	HDD		
Port8	ODD		
Port9	LAN		
Port10	Un-used		

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0 MB-1
PORT-2	NC
PORT-3	Cobime USB3.0 Smaii Board
PORT-4	NC

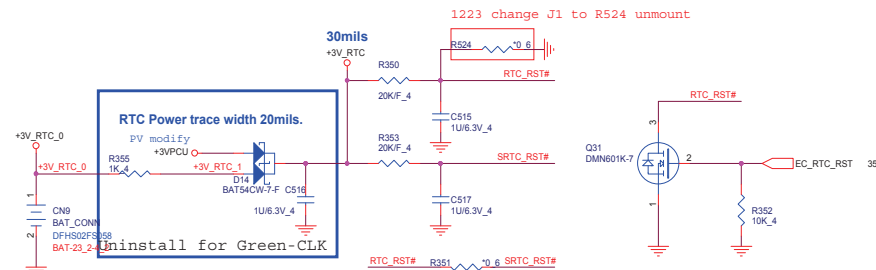
USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	Cobime USB3.0 MB-1
PORT-2	Cobime USB3.0 Smaii Board
PORT-3	Camera
PORT-4	NC
PORT-5	NC
PORT-6	Cobime USB3.0 Smaii Board
PORT-7	WLAN
PORT-8	Touch Screen
PORT-9	NC
PORT-10	NC

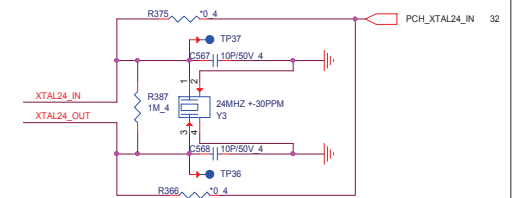


**PROJECT :Y11X-6L**  
**Quanta Computer Inc.**

Size Custom	Document Number 12 - SKYPAKE 16/20 (PCIE/USB)	Rev 1A
Date: Wednesday, May 06, 2015	Sheet 12of	49



The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.



0305  
Change C567 and C568 to 10pf



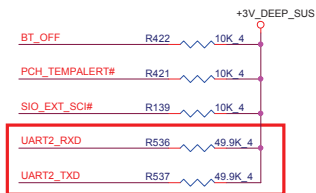
<p><b>PROJECT :Y11X-6L</b>          Quanta Computer Inc.</p>
--

Size Custom	Document Number <b>13 -- SKYPAKE 17/20 (CLK)</b>	Rev 1A
Date: Wednesday, May 06, 2015	Sheet	13 of 40



## Skylake (GPIO)

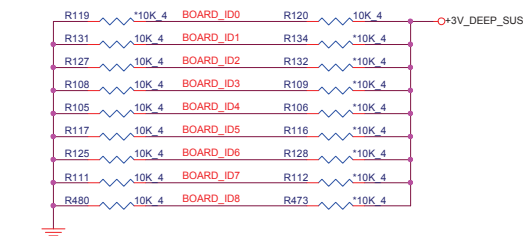
+3V 2,4,10,11,12,13,15,16,17,18,20,27,28,29,30,31,32,33,34,35,41,43,44  
+3V\_DEEP\_SUS 4,10,11,12,15,16,18



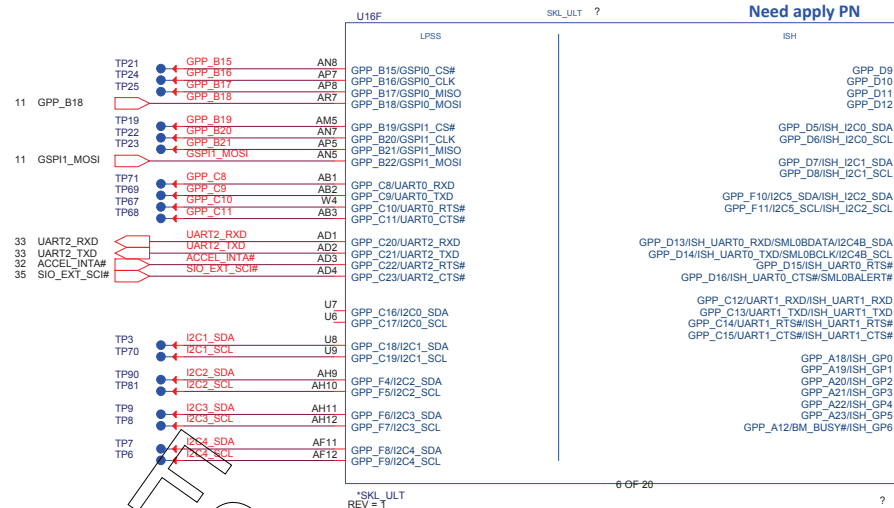
1227 Add R536 and R537 for  
UART2 function reserved



1223 Add R525



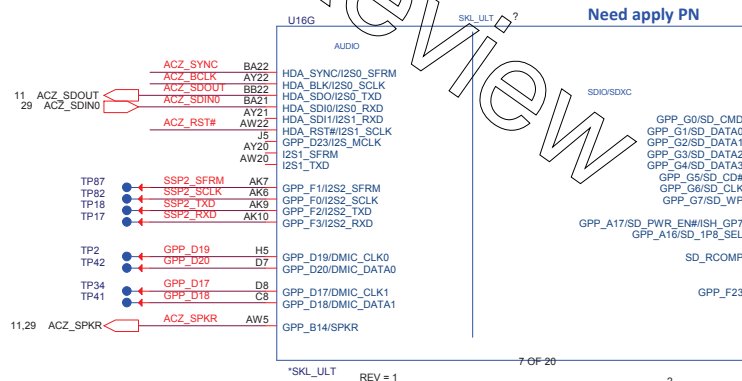
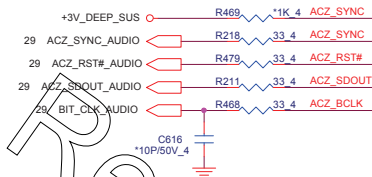
Skylake U	BOARD_ID[8:7]	BOARD_ID[6:5]	Board ID [4:3]	BOARD_ID[2:1]	BOARD_ID0
Model	ID8 ID7	ID6 ID5	ID4 ID3	ID2 ID1	ID0
Definition	Reserve (Default = 00)	Reserve (Default = 00)	00 Single Rank (X1B) 01 Dual Rank (X1B) 10 Meso-AMD (X1A) 11 Reserve	00 14" 01 15" 10 17" 11 Reserve	0 : UMA 1 : DIS



0224  
Unmount R547  
0114  
Del TP57, Add R547 with 0ohm

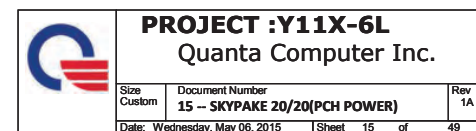
0305  
Del TP73

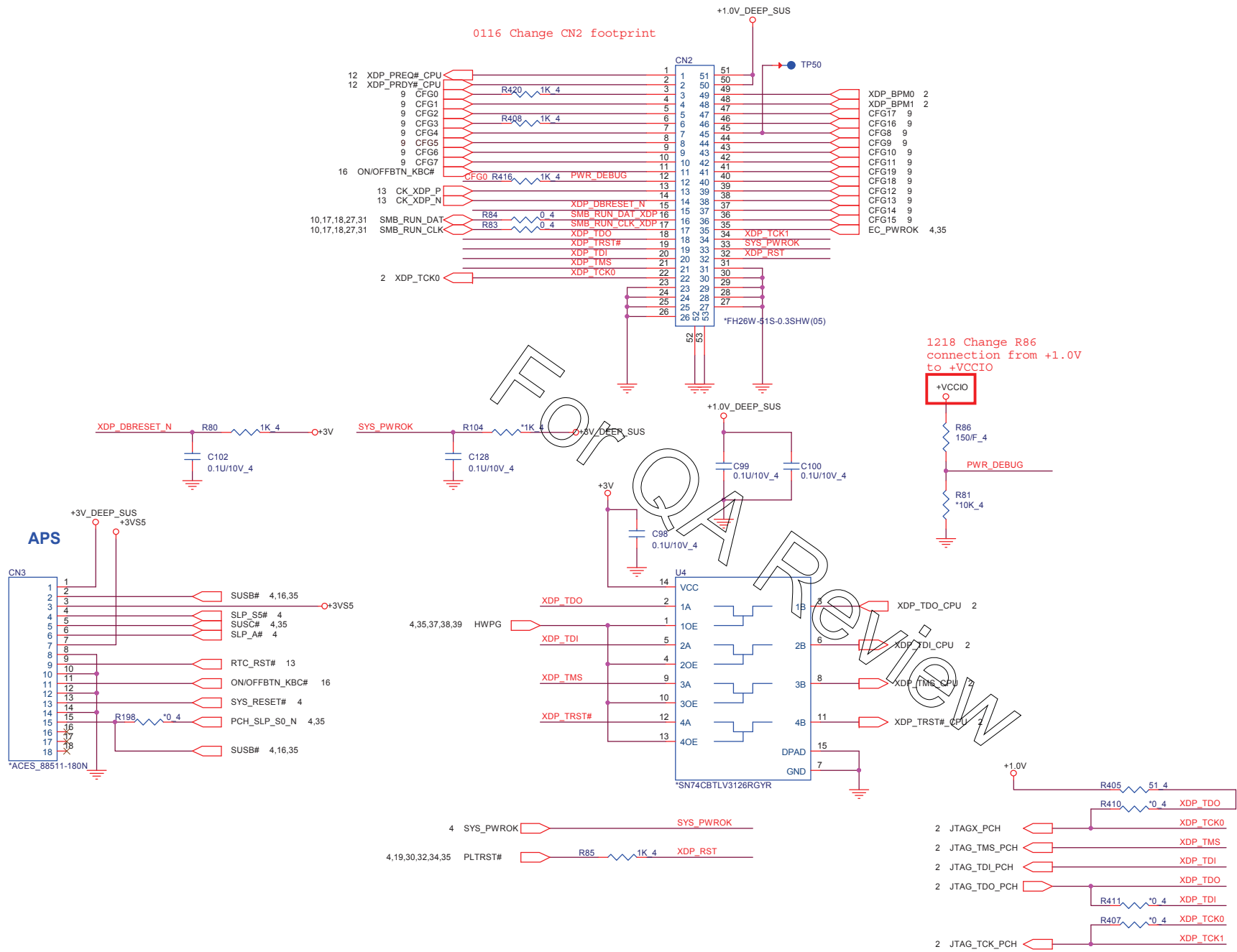
## HDA Bus(CLG)

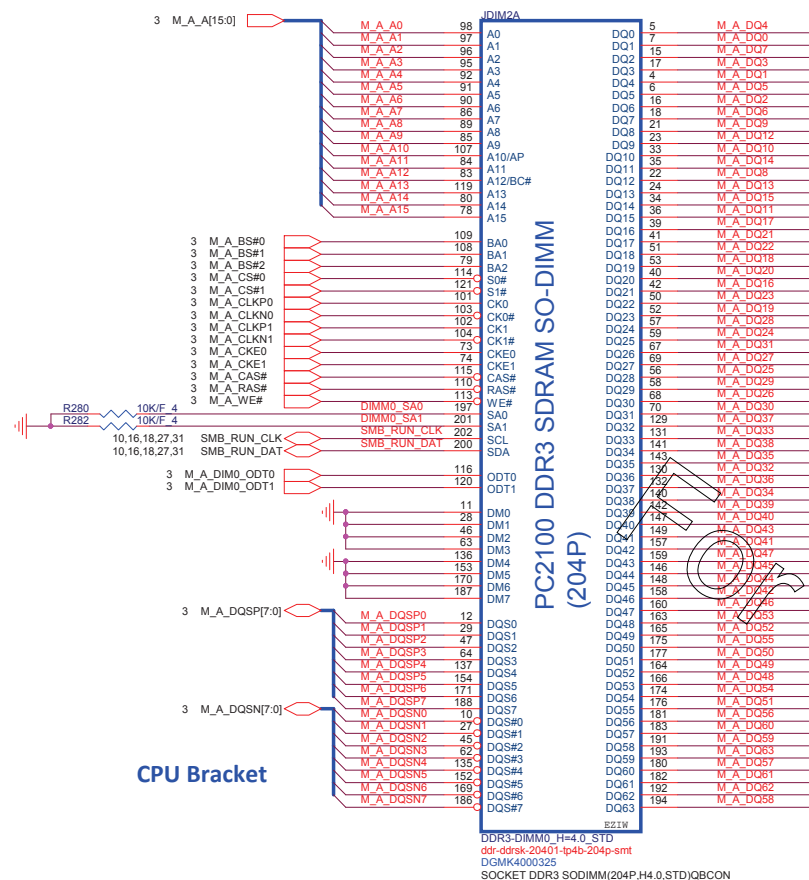


PROJECT :Y11X-6L  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	14 -- SKYPAKE 19/20 (GPIO)	1A
Date: Wednesday, May 06, 2015	Sheet 14 of 49	



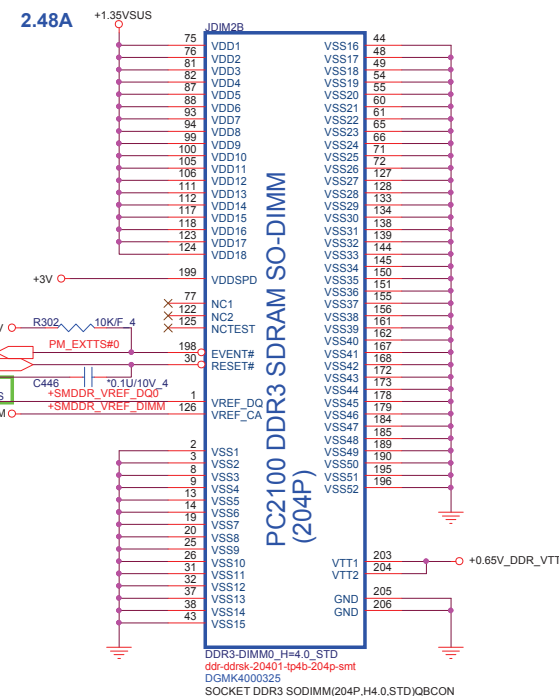




CPU Bracket

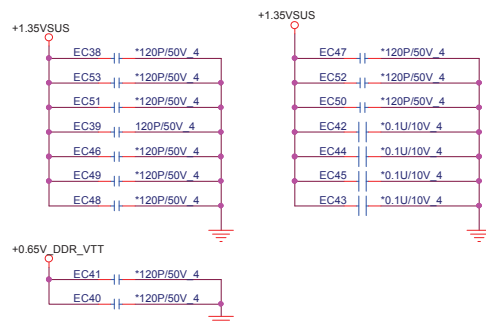
M\_A\_DQ[63:0] 3

PV modify to short pad



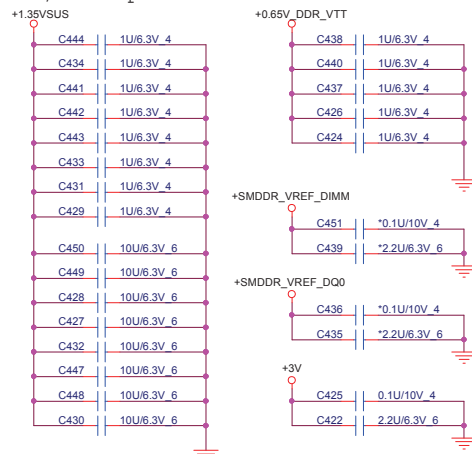
2,4,10,11,12,13,14,15,16,18,20,27,28,29,30,31,32,33,34,35,41,43,44 +3V  
3,6,18,38,40,46 +1.35VSUS  
18,38 +0.65V\_DDR\_VTT  
18 +SMDDR\_VREF\_DIMM

## For EMI RESERVE

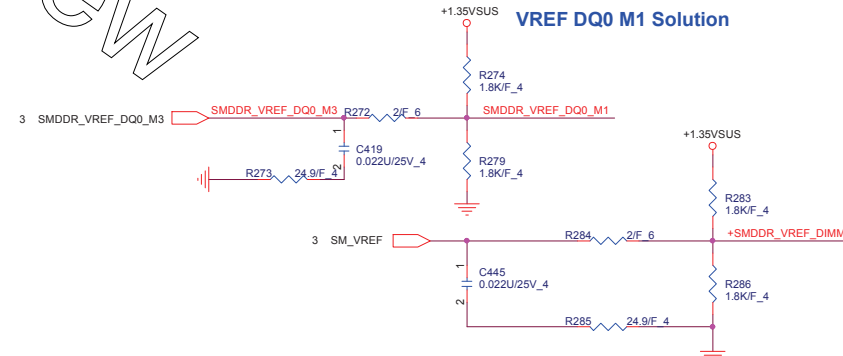


## Place these Caps near So-Dimm0.

1uF/10uF 4pcs on each side of connector



## VREF DQ0 M1 Solution

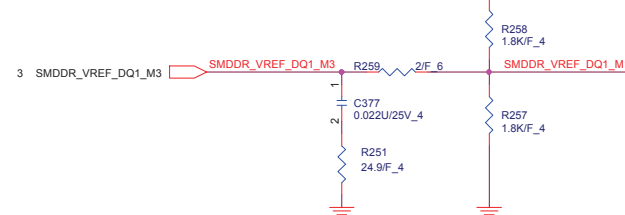
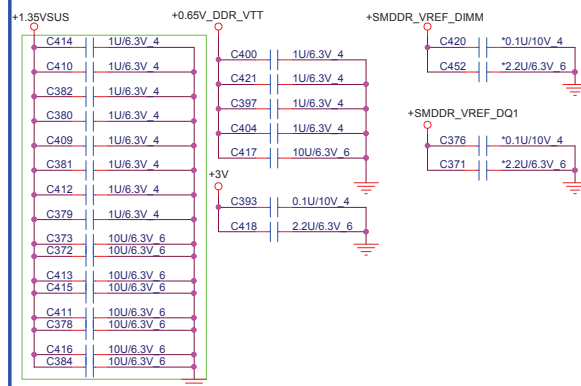


**PROJECT :Y11X-6L**  
**Quanta Computer Inc.**

Size Custom	Document Number 17 - DDR3 DIMM0-STD(4.0H)	Rev 1A
Date: Wednesday, May 06, 2015	Sheet	17 of 49

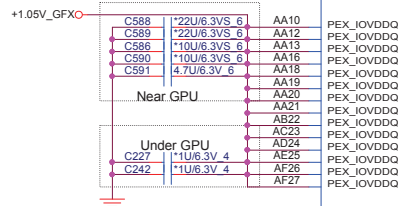


1uF/10uF 4pcs on each side of connector

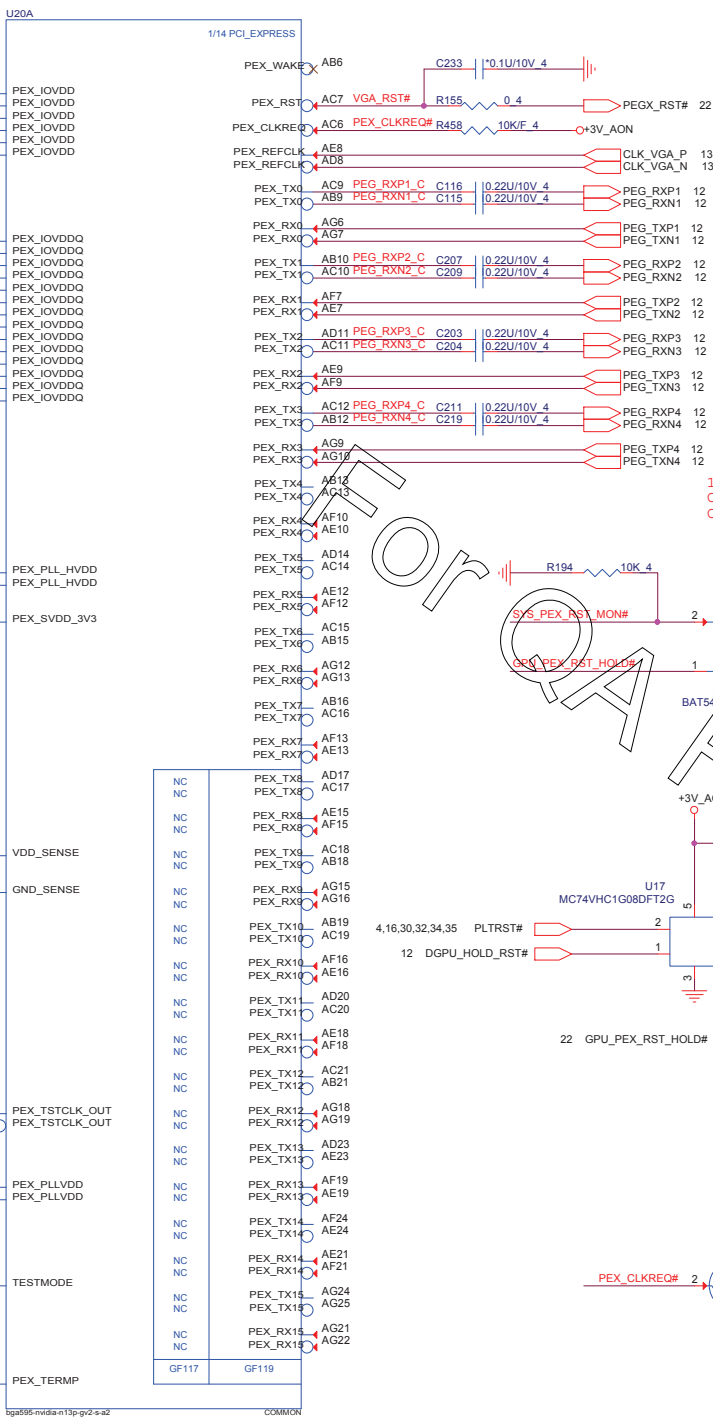
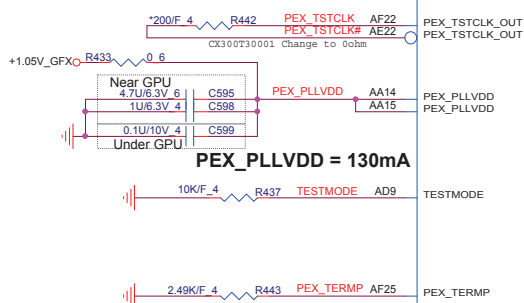
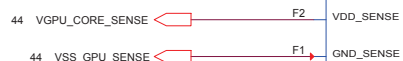
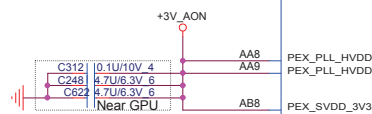




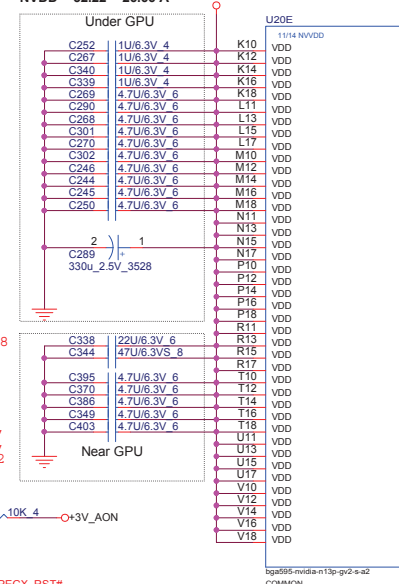
```
1230 Change C587
size to 0603
```

$$\text{PEX IOVDD} + \text{PEX IOVDDQ} = 1.042\text{A}$$


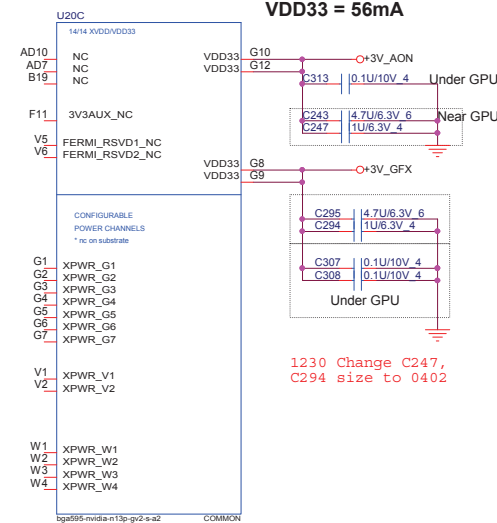
PEX\_PLL\_HVDD +  
PEX\_SVDD 3V3 = 143mA



NVDD = 32.22 ~ 26.66 A +VGACORE



VDD33 = 56mA

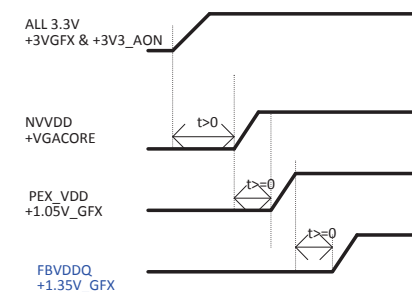


1230 Change C338  
size to 0603

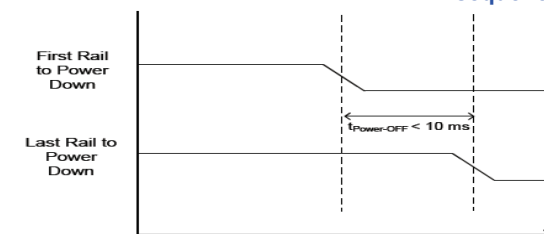
```
1230 Change C395,  
C370, C386, C349,  
C403 size to 0402
```

1230 Change C247,  
C294 size to 0402

## Power up sequence



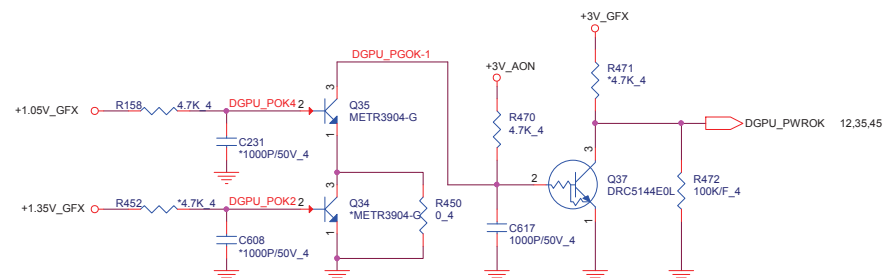
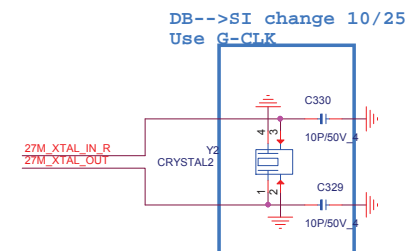
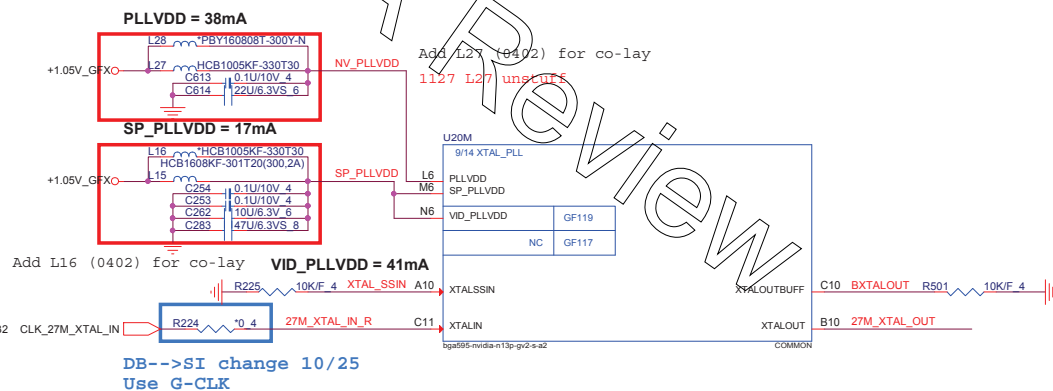
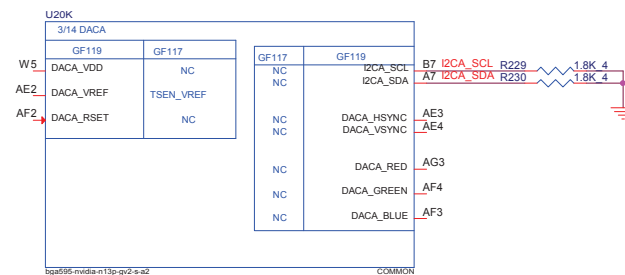
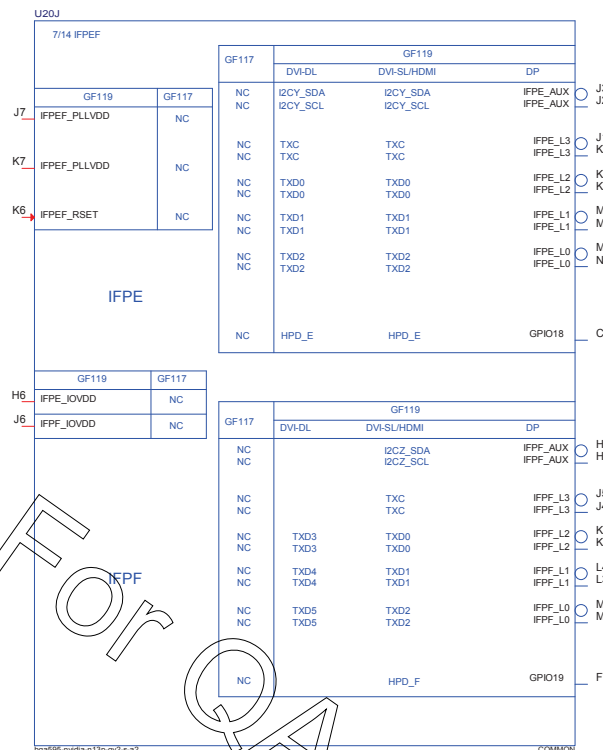
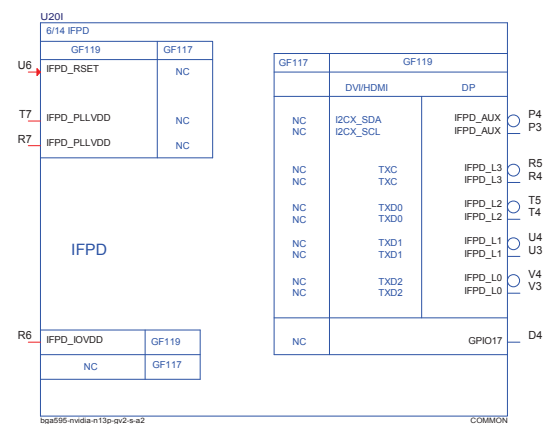
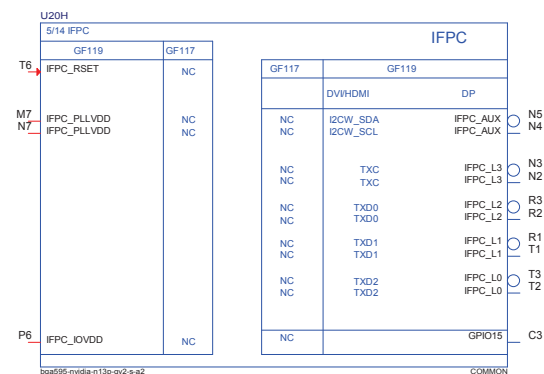
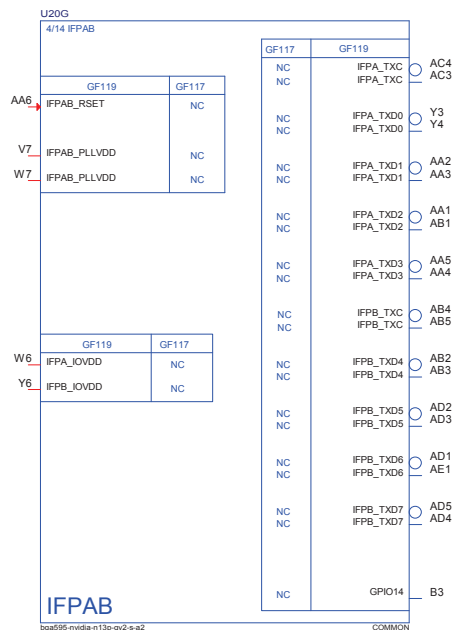
## Power down sequence



**PROJECT :Y11X-6L**  
Quanta Computer Inc.

Size Custom	Document Number <b>19 – N15S-GT (PCIE I/F) /NVDD</b>	Rev 1A
Date: Wednesday, May 06, 2015		Sheet 19 of 49





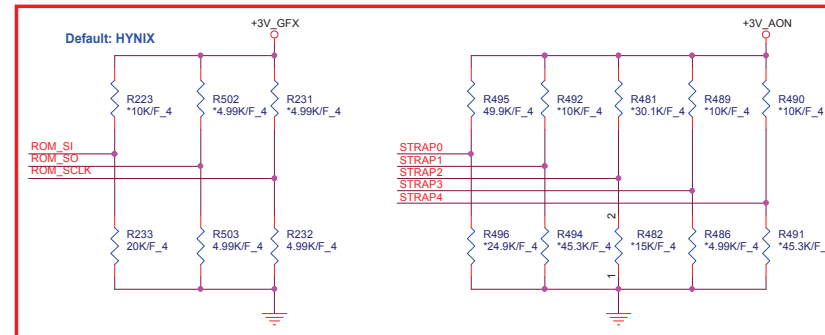
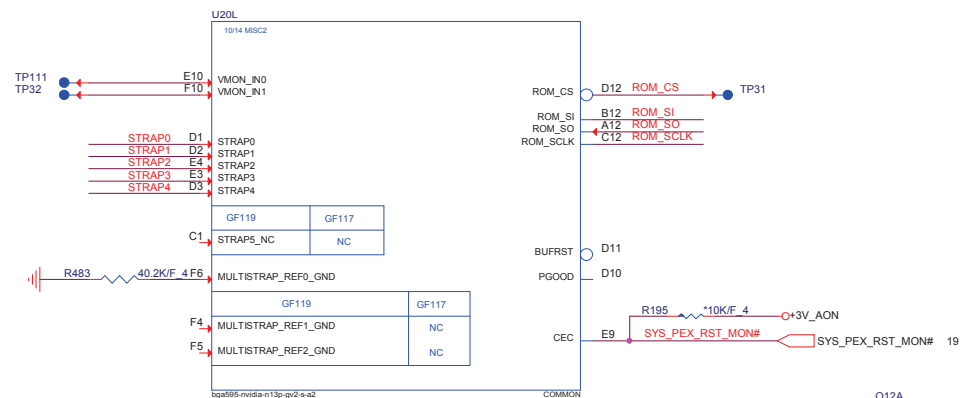
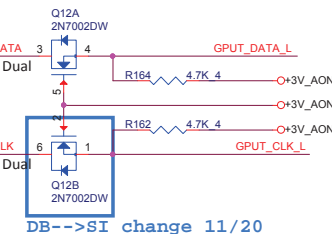
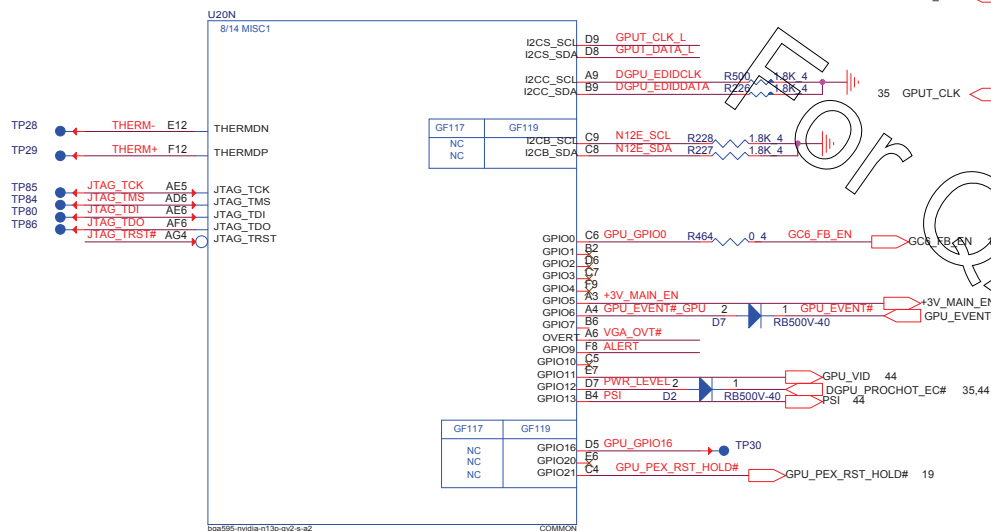


Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111



VRAM Configuration Table

RAMCFG (3:0)	DESCRIPTION	Vendor	Vendor P/N	Strapping	TOP B/S	QBC
0000	DDR3L 256Mx16, 64bit, 4Gb, 900MHz	HYNIX	H5TC4G63CFR-N0C	0x2	AKD5PZDTW01	AKD5PZDTW02
0010	DDR3L 256Mx16, 64bit, 4Gb, 900MHz	Micron	MT41J256M16HA-093G:E	0x4	AKD5PZSTL00	AKD5PZSTL01
0100	DDR3L 256Mx16, 64bit, 4Gb, 900MHz	SAMSUNG	K4W4G1646E-BC1A	0x1	AKD5PGDT500	AKD5PGDT501
0001	DDR3L 256Mx16, 64bit, 4Gb, 900MHz					

## GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding



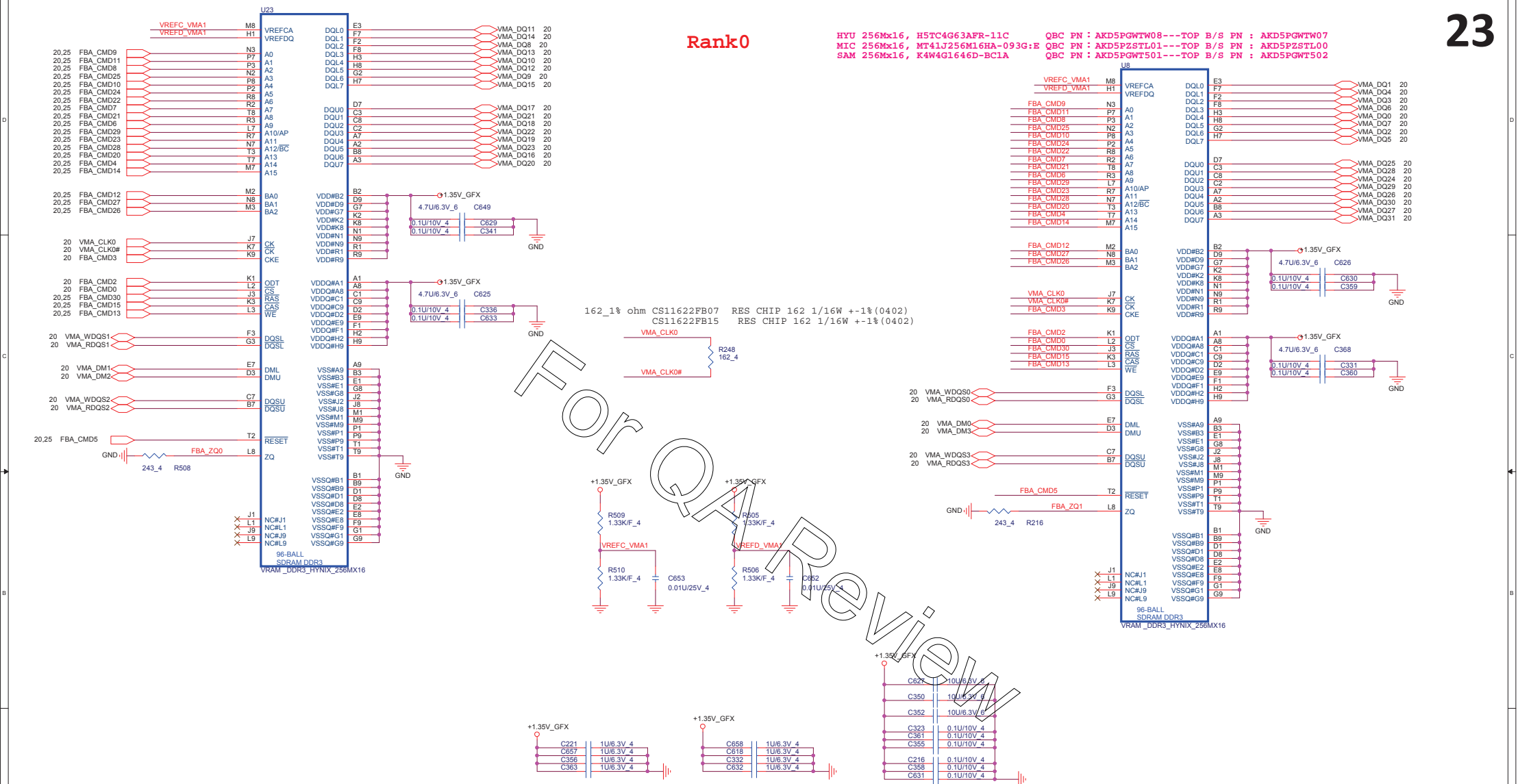
**PROJECT :Y11X-6L**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	22 - N15S-GT (GPIO/STRAPS)	1A
Date: Wednesday, May 06, 2015	Sheet 22 of 49	

## Rank0


HYU 256Mx16, H5TC4G63AFR-11C  
MIC 256Mx16, MT41J256M16HA-093G:E  
SAM 256Mx16, K4W4G1646D-BC1A

QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07  
E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00  
QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502






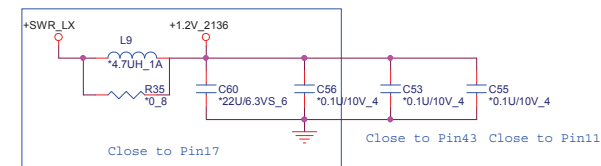
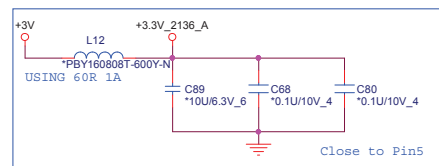
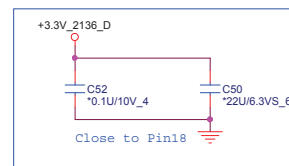
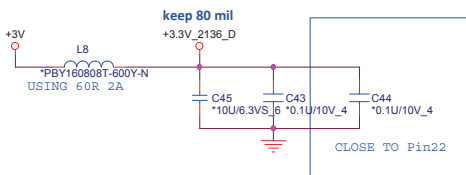
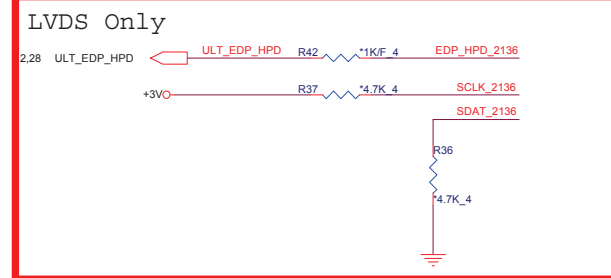
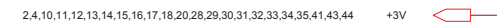
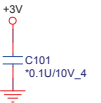
For QA Review

			<b>PROJECT :Y11X-6L</b> Quanta Computer Inc.		
Size Custom	Document Number <b>24 -- Reserve</b>				Rev 1A
Date: Wednesday, May 06, 2015			Sheet	24	of 49



For QA Review

			<b>PROJECT :Y11X-6L</b> Quanta Computer Inc.		
Size Custom	Document Number <b>26 -- Reserve</b>				Rev 1A
Date: Wednesday, May 06, 2015			Sheet	26	of 49



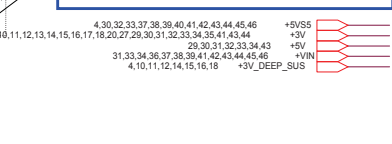
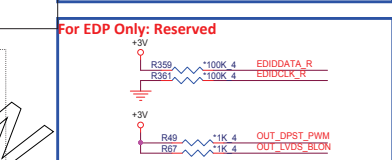
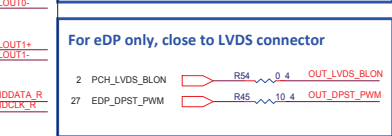
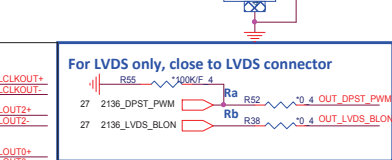
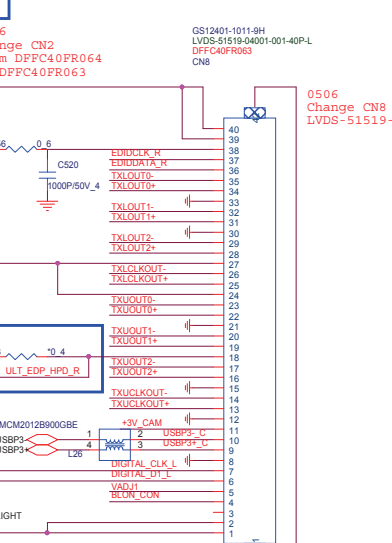
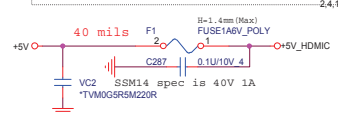
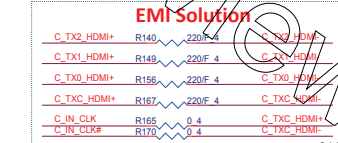
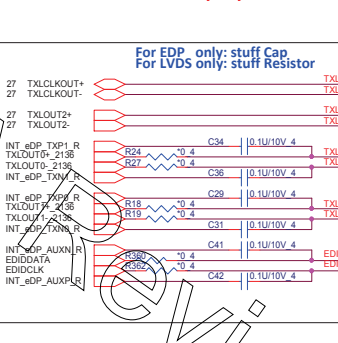
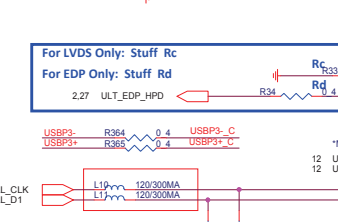
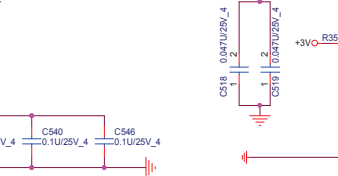
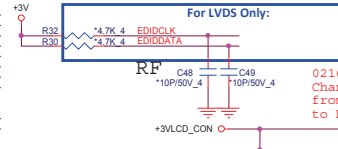
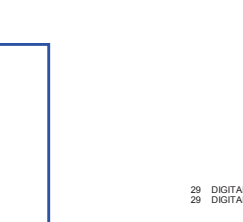
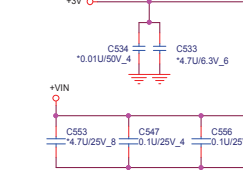
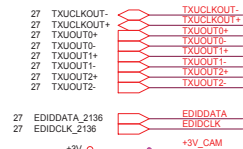
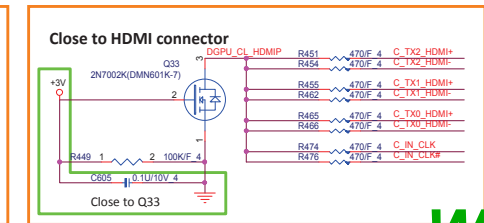
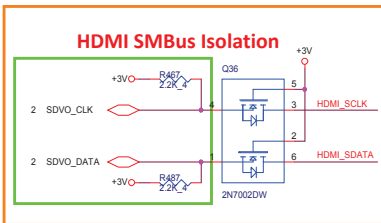
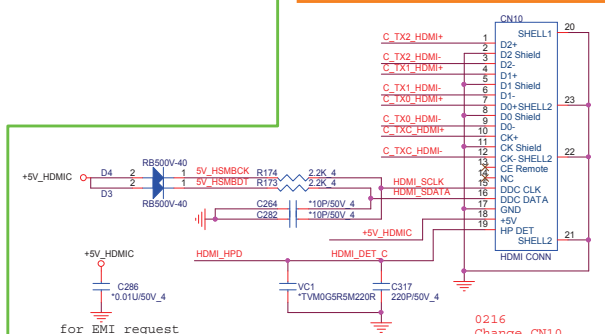
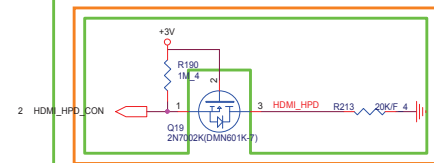
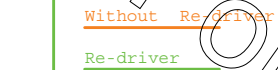
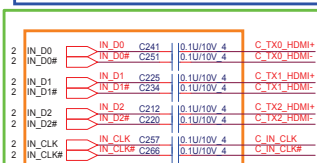
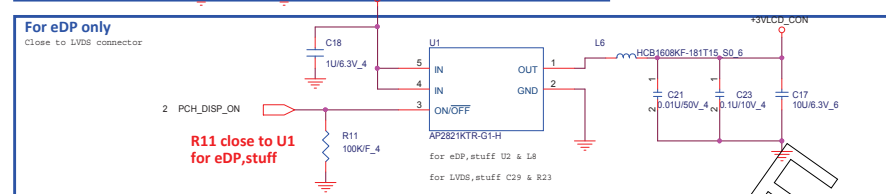
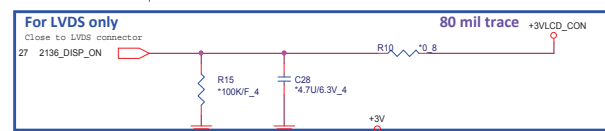
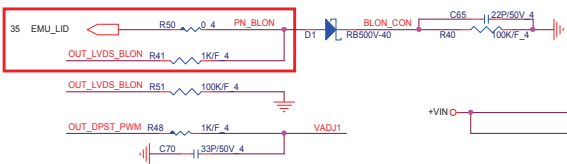
SWR MODE	LDO MODE
Stuff L9	Stuff R35



**PROJECT :Y11X-6L**  
Quanta Computer Inc.

Size Custom	Document Number <b>27 – RTD2136</b>	Rev 1A
Date: Wednesday, May 06, 2015		Sheet 27 of 49

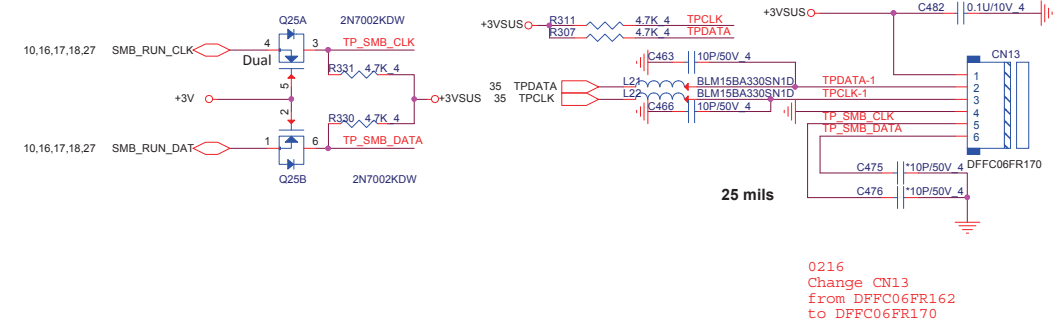
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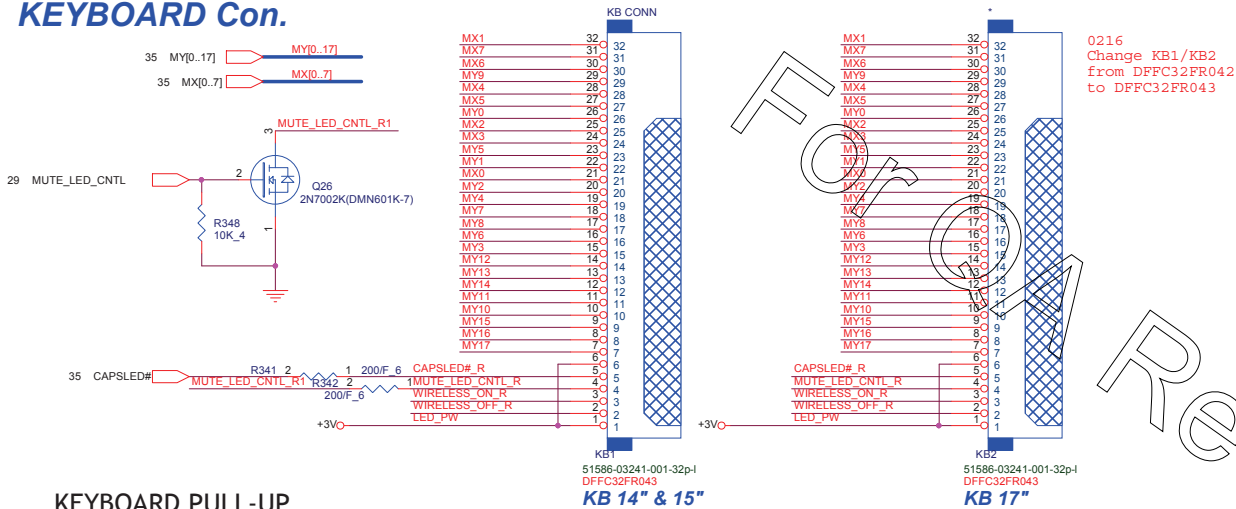




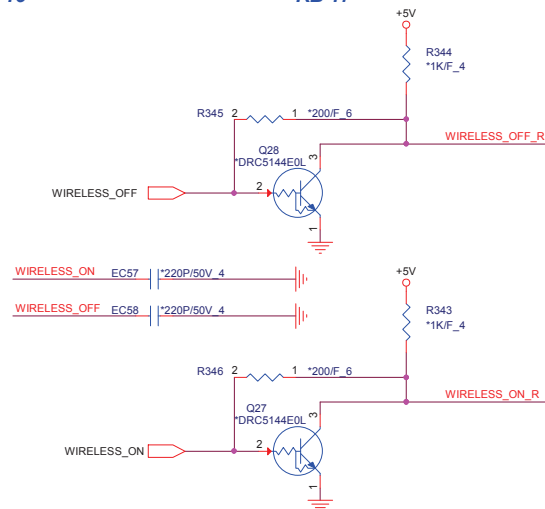
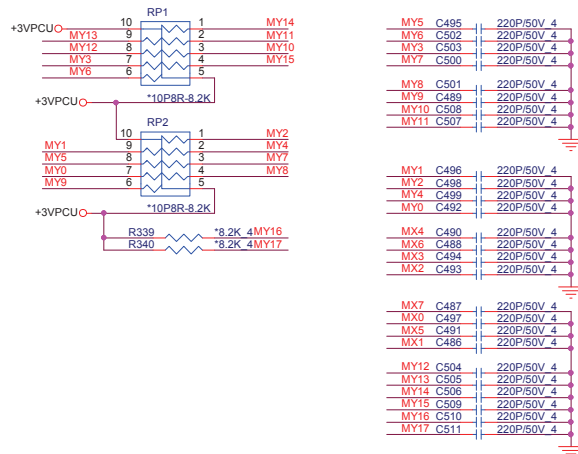




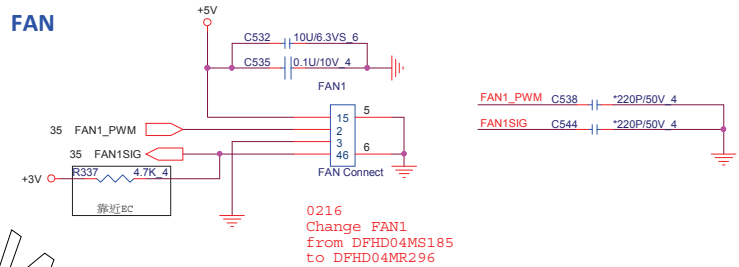
## KEYBOARD Con.



## KEYBOARD PULL-UP



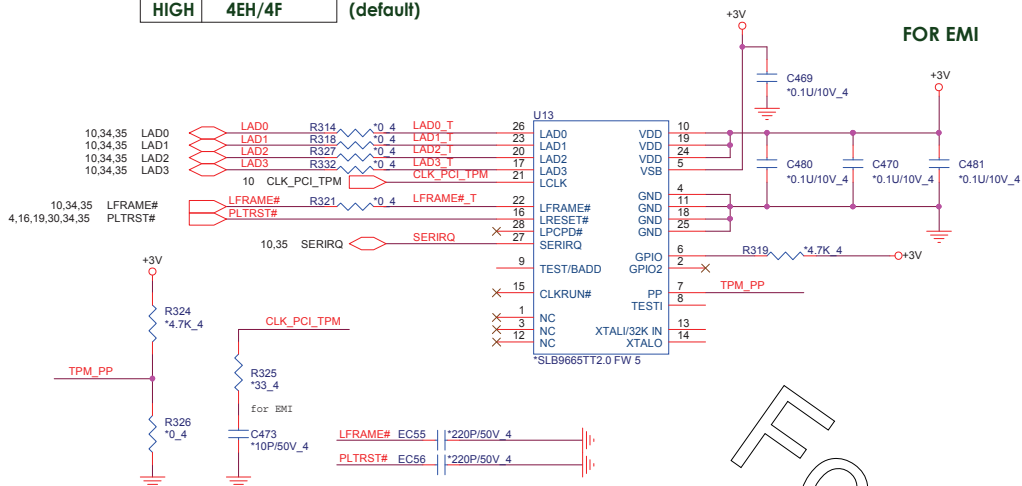
## FAN



## TPM (2.0)

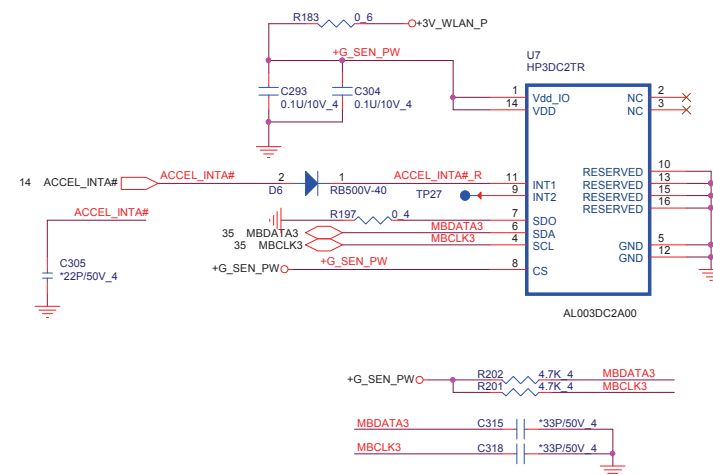
Address

	BADD
HIGH	4EH/4F (default)

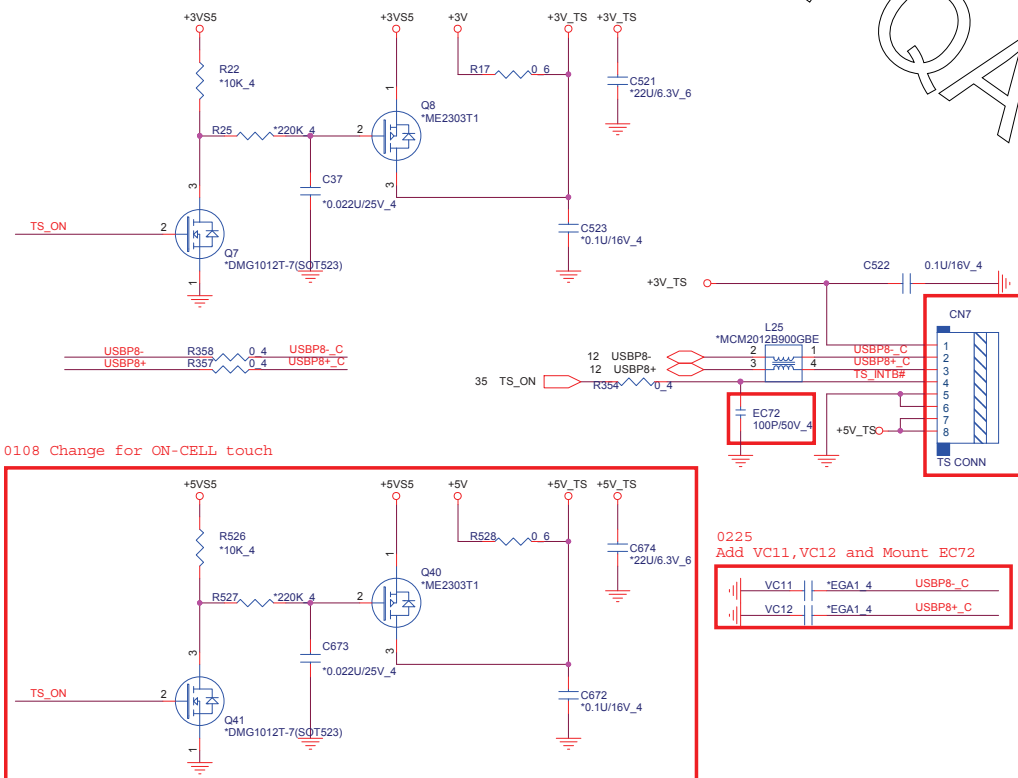


## Accelerometer Sensor

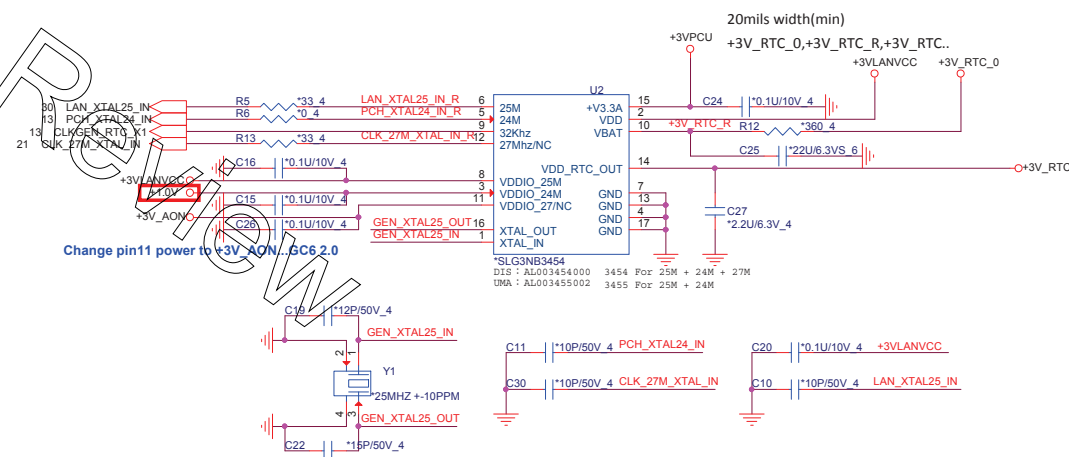
G-Sensor Power need check



## Touch screen

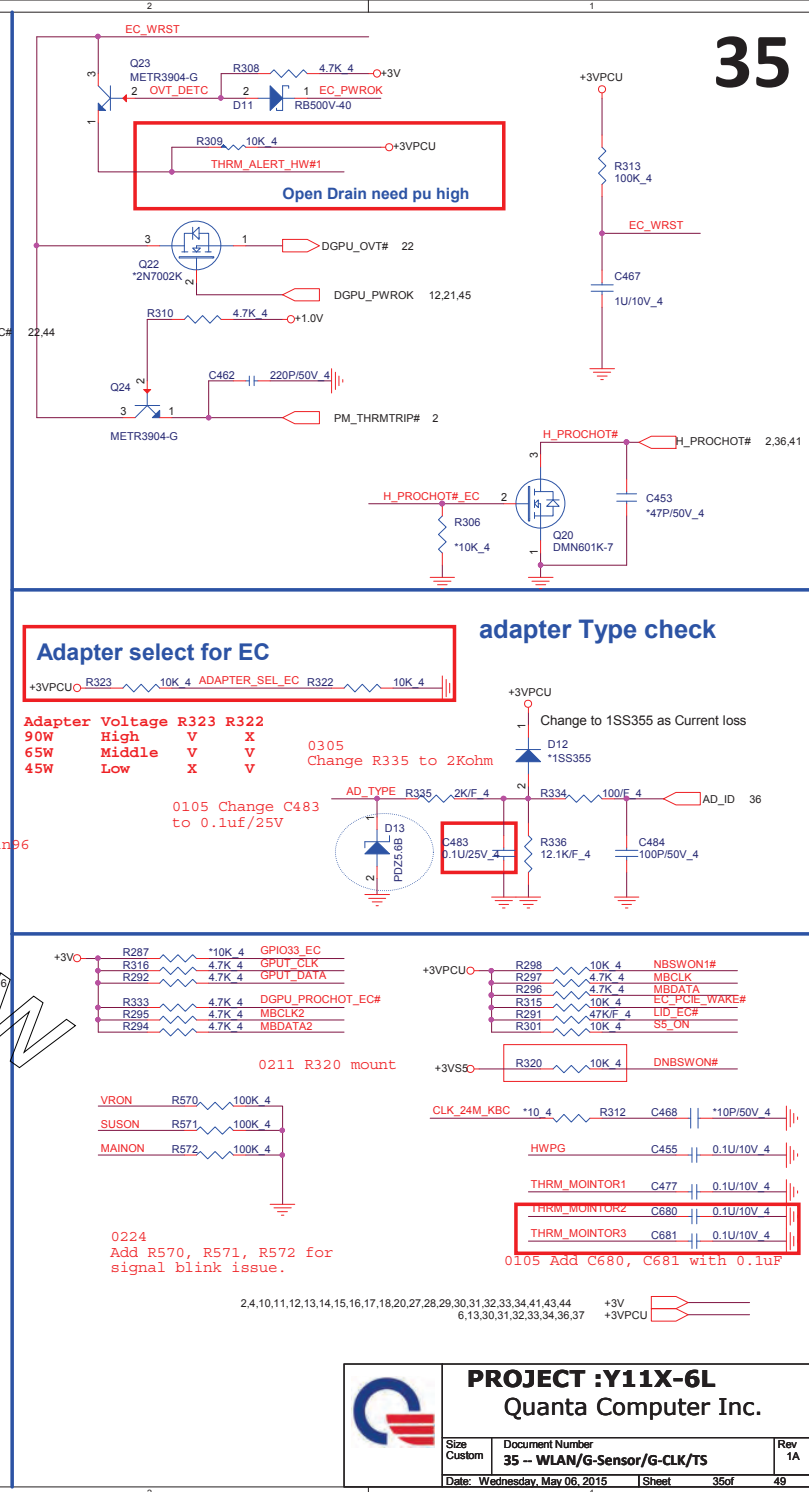


## Green CLK Circuitry













**WWW.AliSaler.Com**



2014/12/18 updated

**Do Not add test pad on VCC & LDO pin**

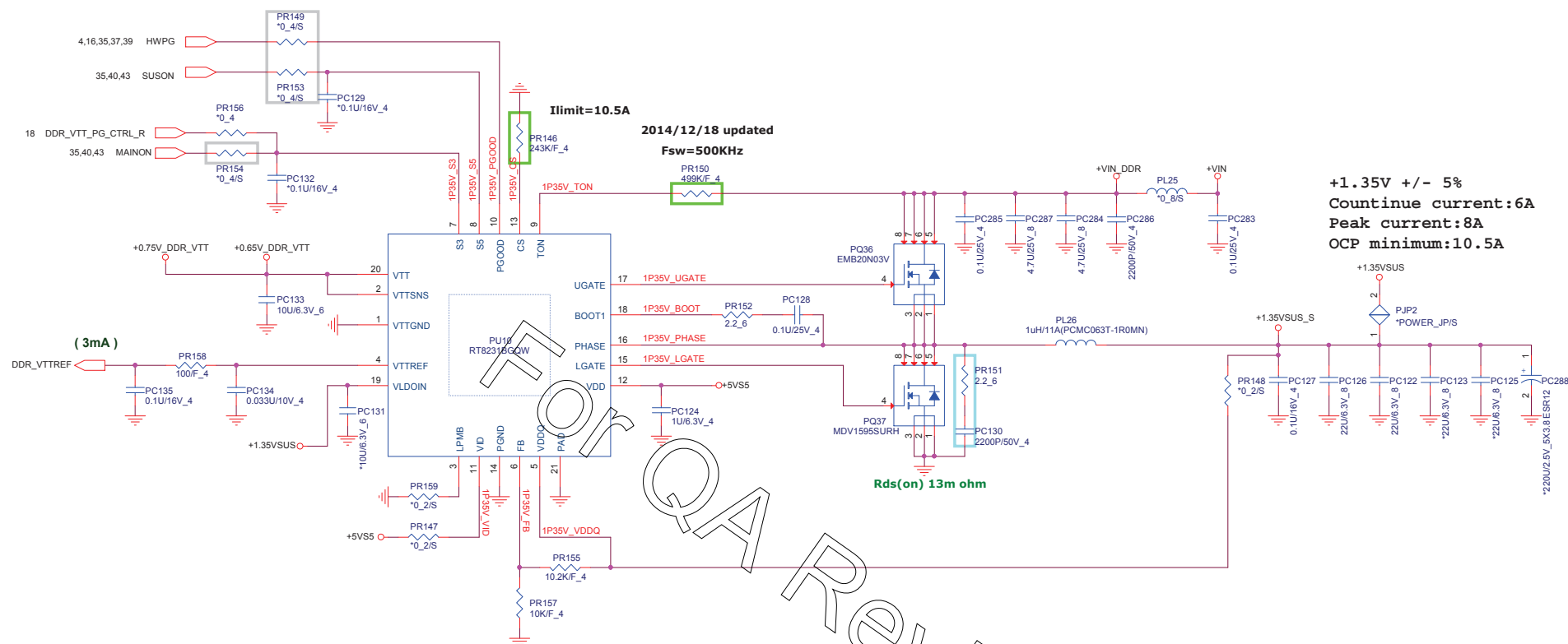
USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff


**Do Not add test pad on VCC & LDO pin**

**+5 Volt +/- 5%**  
**TDC: 8A**  
**EDP: 9A**

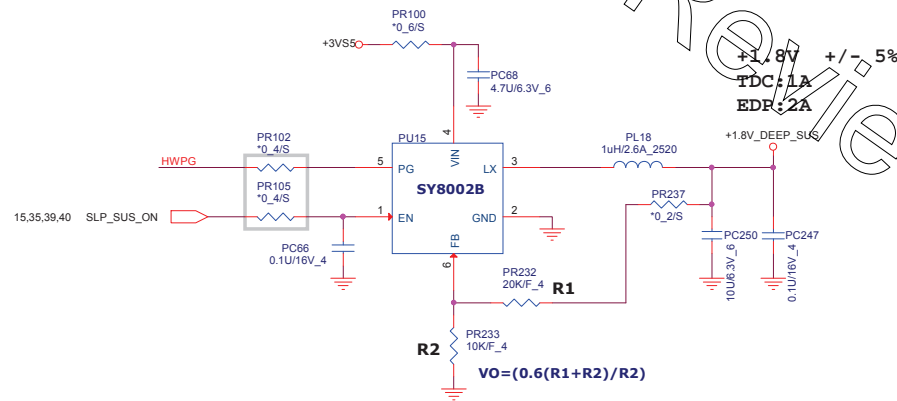
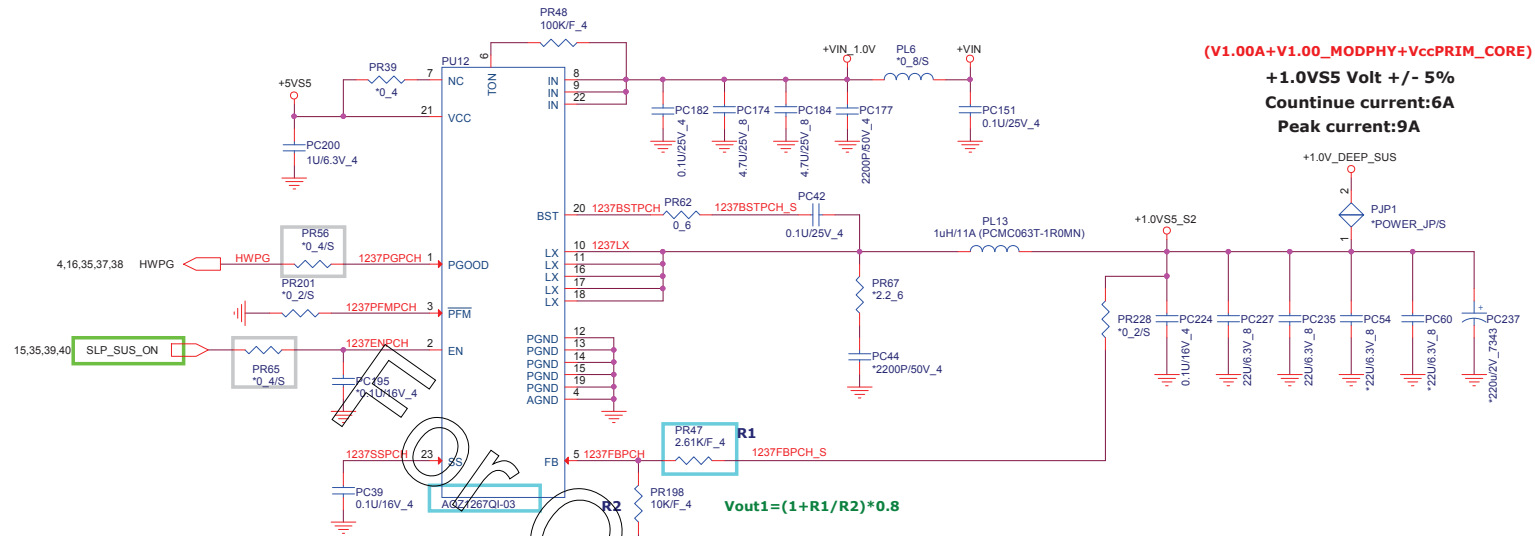
USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff

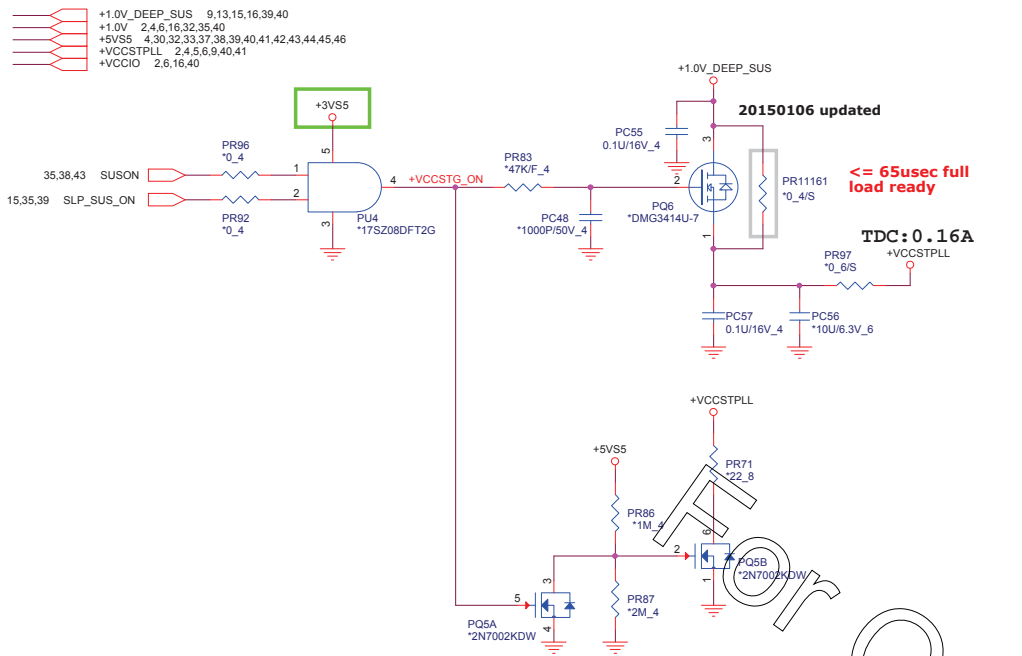
**Do Not add test pad on VCC & LDO pin**



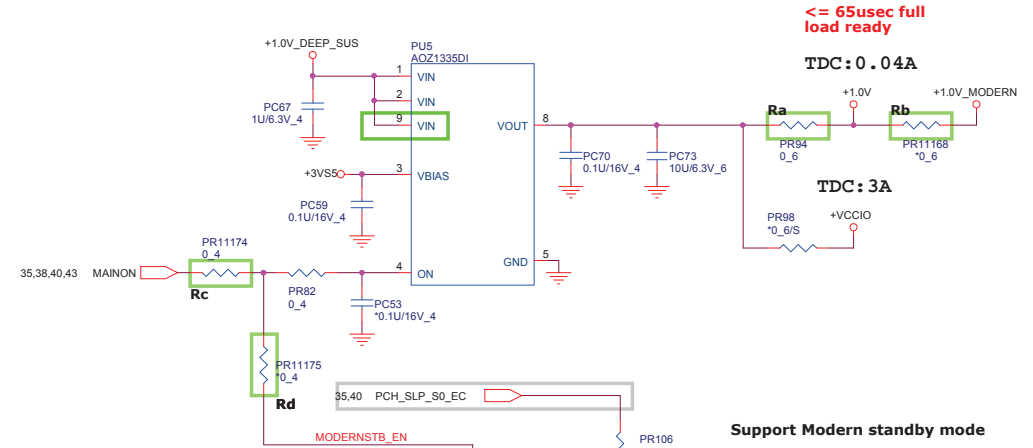
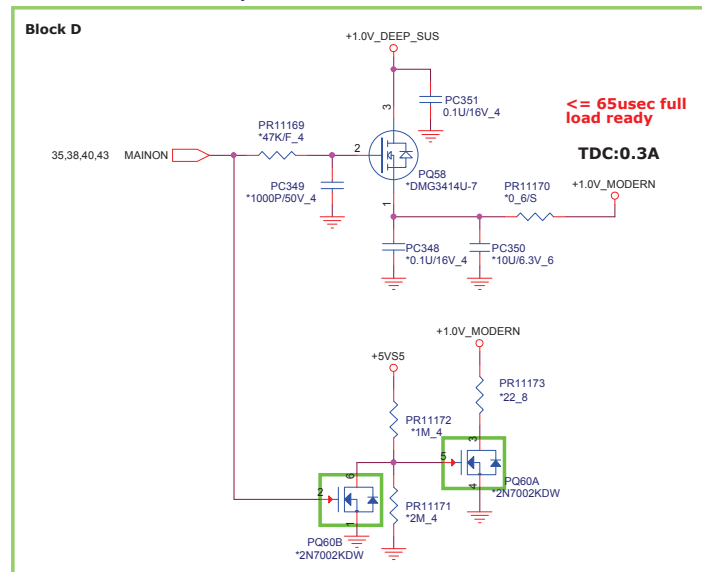
	<b>PROJECT :Y11X-6L</b> Quanta Computer Inc.		
	Size Custom	Document Number <b>DDR3 (RT8231B)</b>	Rev <b>1A</b>
	Date: Wednesday, May 06, 2015	Sheet	38 of 49

+VIN 28,31,33,34,36,37,38,41,42,43,44,45,46  
 +5VS5 4,30,32,33,37,38,40,41,42,43,44,45,46  
 +3VS5 4,10,15,16,32,34,35,37,40,43,46  
 +1.8V\_DEEP\_SUS 9,15  
 +1.0V\_DEEP\_SUS 9,13,15,16,40



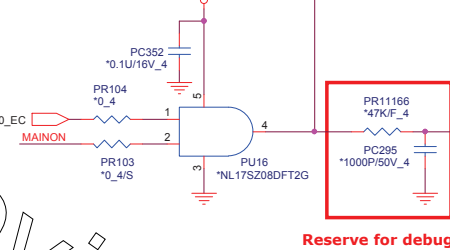


### Reserve for Modern StandBy




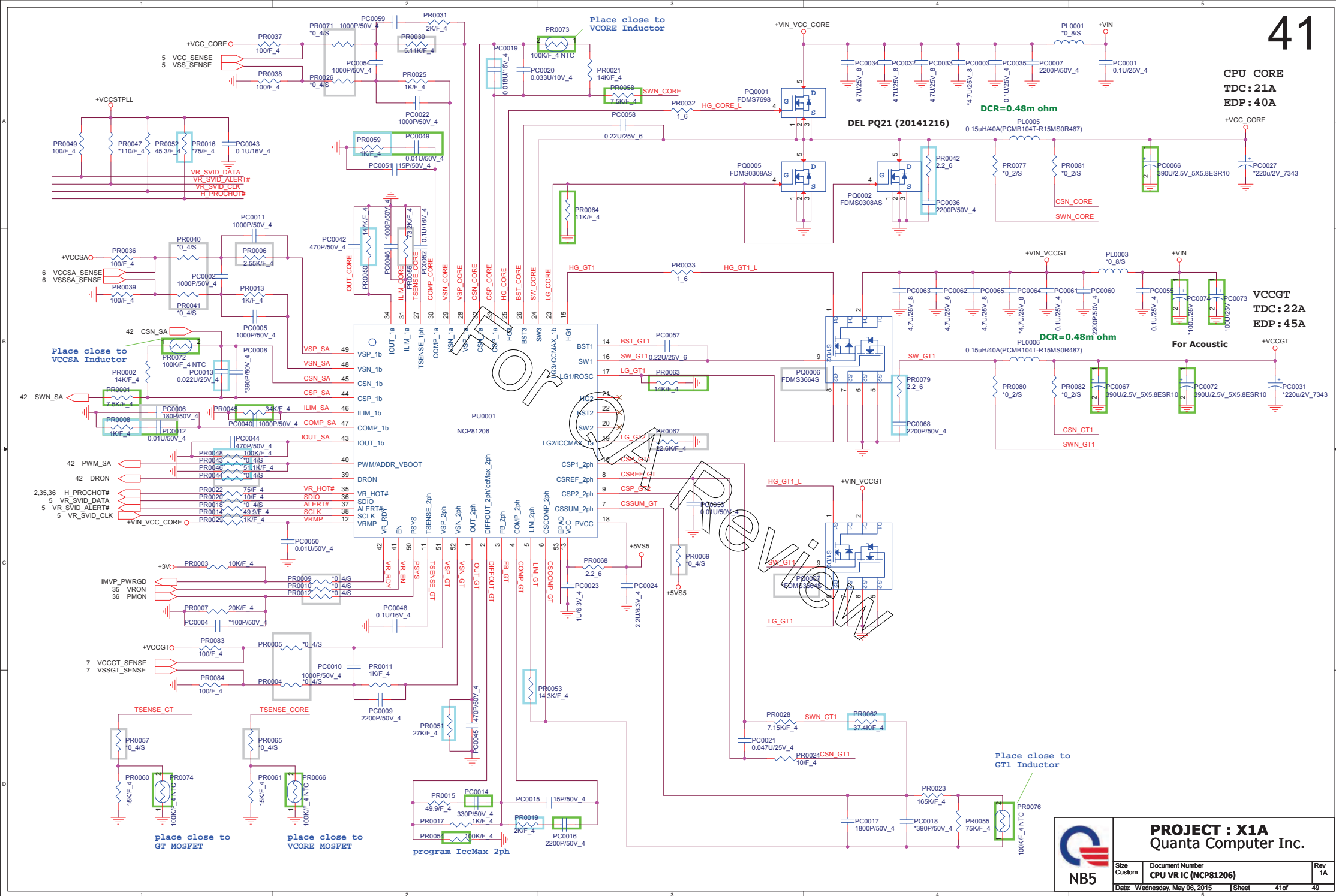
### Reserve for Modern StandBy

#### Block C



+1.0V 2,4,6,16,32,35,40  
 +3VS5 4,10,15,16,32,34,35,37,39,43,46  
 +5VS5 4,30,32,33,37,38,39,40,41,42,43,44,45,46  
 +VCCIO 2,6,16,40  
 +1.35VSUS 3,6,17,18,38,46  
 +VCCSTPLL 2,4,5,6,9,40,41  
 +1.0V\_MODERN 2,4,5,6,9,40,41  
 +1.0V\_DEEP\_SUS 9,13,15,16,39,40  
 +1.35V\_VCCPLL\_OC 6

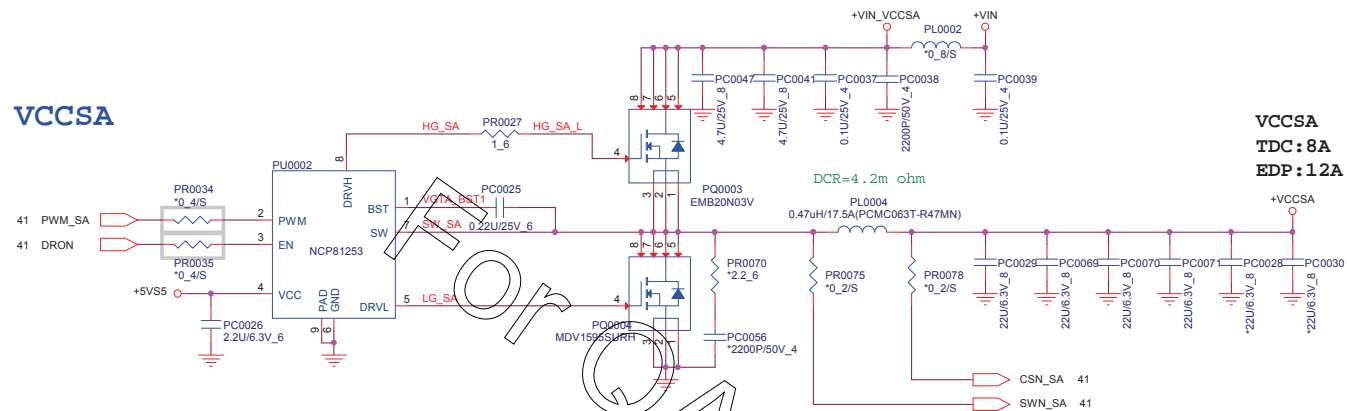
 <b>PROJECT :Y11X-6L</b> Quanta Computer Inc.		
Size Custom	Document Number <b>+1.0V/+VCCSTPLL</b>	Rev 1A
Date: Wednesday, May 06, 2015	Sheet 40 of 49	

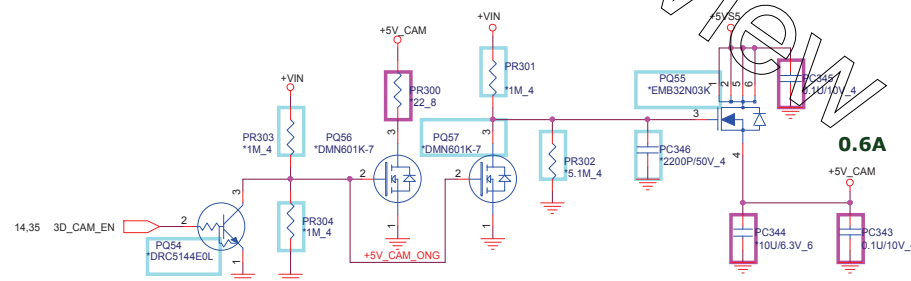
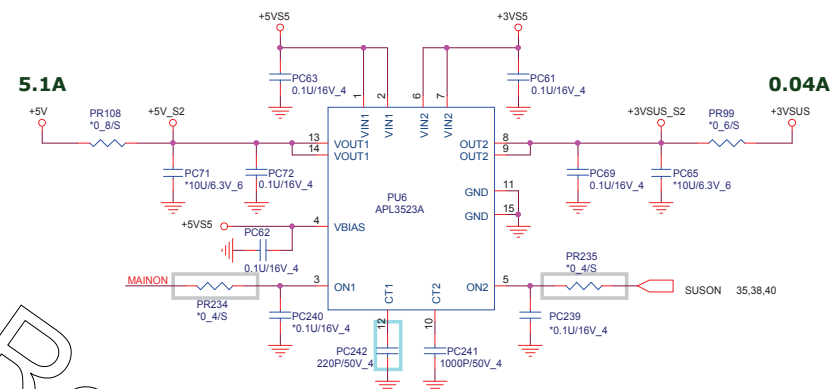


**PROJECT : X1A**  
Quanta Computer Inc.

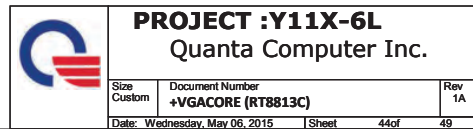
Size	Document Number	Rev
Custom	CPU VR IC (NCP81206)	1A
Date: Wednesday, May 06, 2015	Sheet	41 of 49

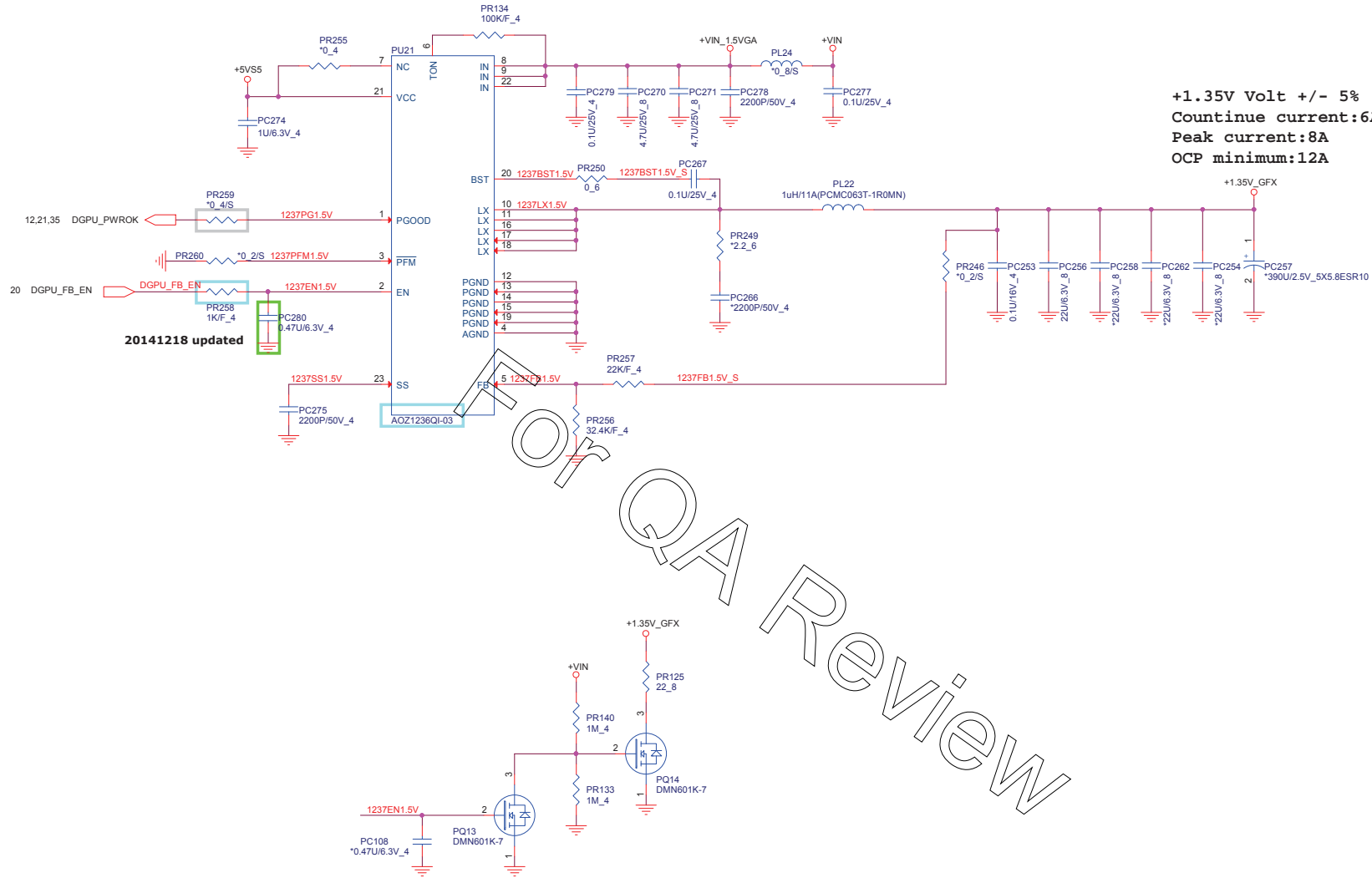




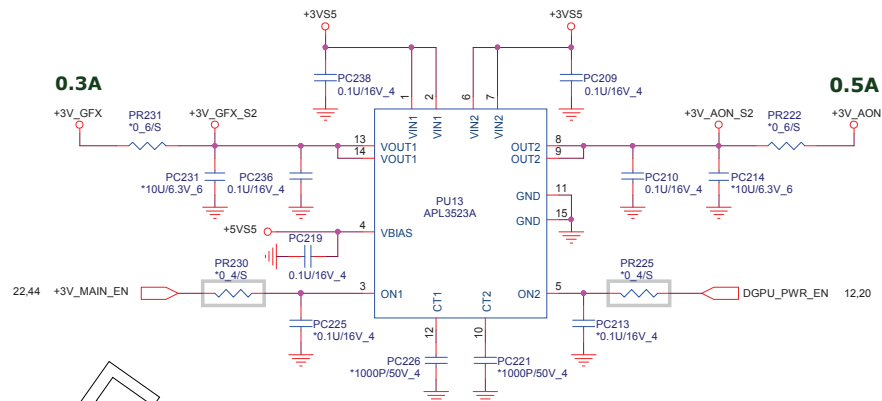
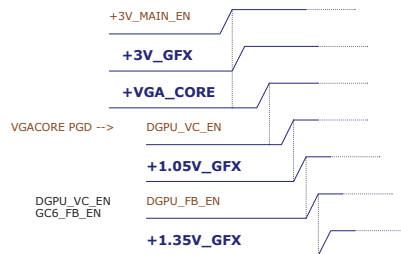


2,4,10,11,12,13,14,15,16,17,18,20,27,28,29,30,31,32,33,34,35,41,44 +3V  
28,29,30,31,32,33,34 +5V  
28,31,33,34,36,37,38,39,41,42,44,45,46 +VIN  
4,10,15,16,32,34,35,37,39,40,46 +3VS5  
4,30,32,33,37,38,39,40,41,42,44,45,46 +5VS5  
30,32 +3V1ANVCC

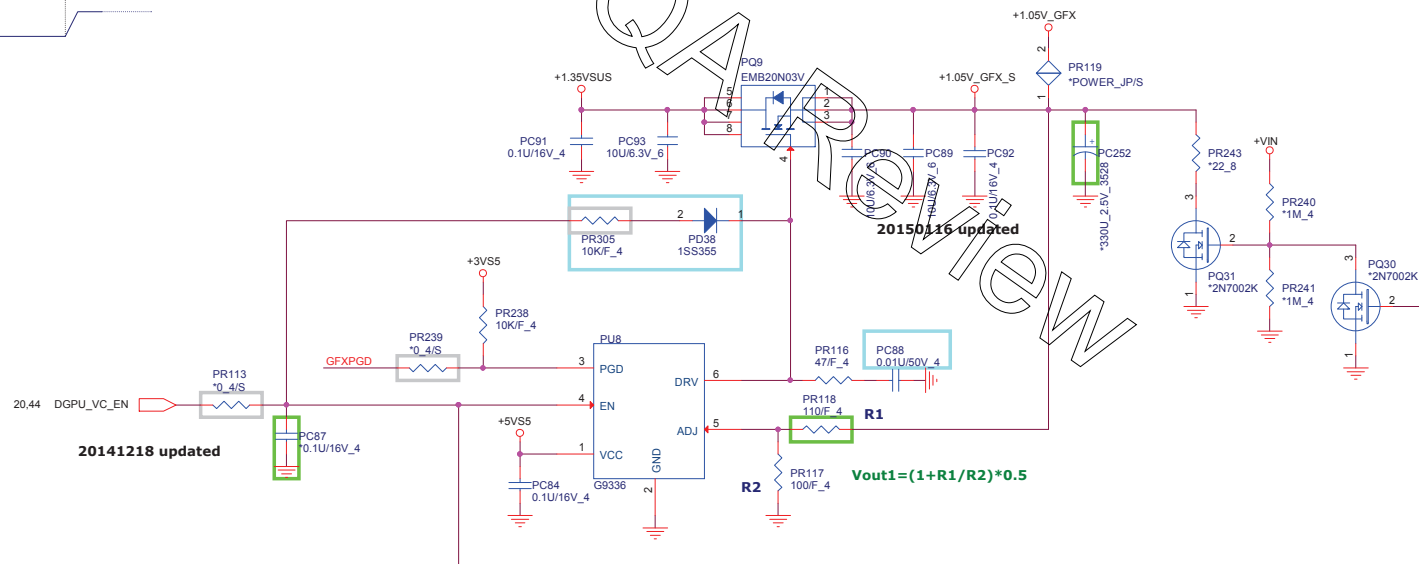




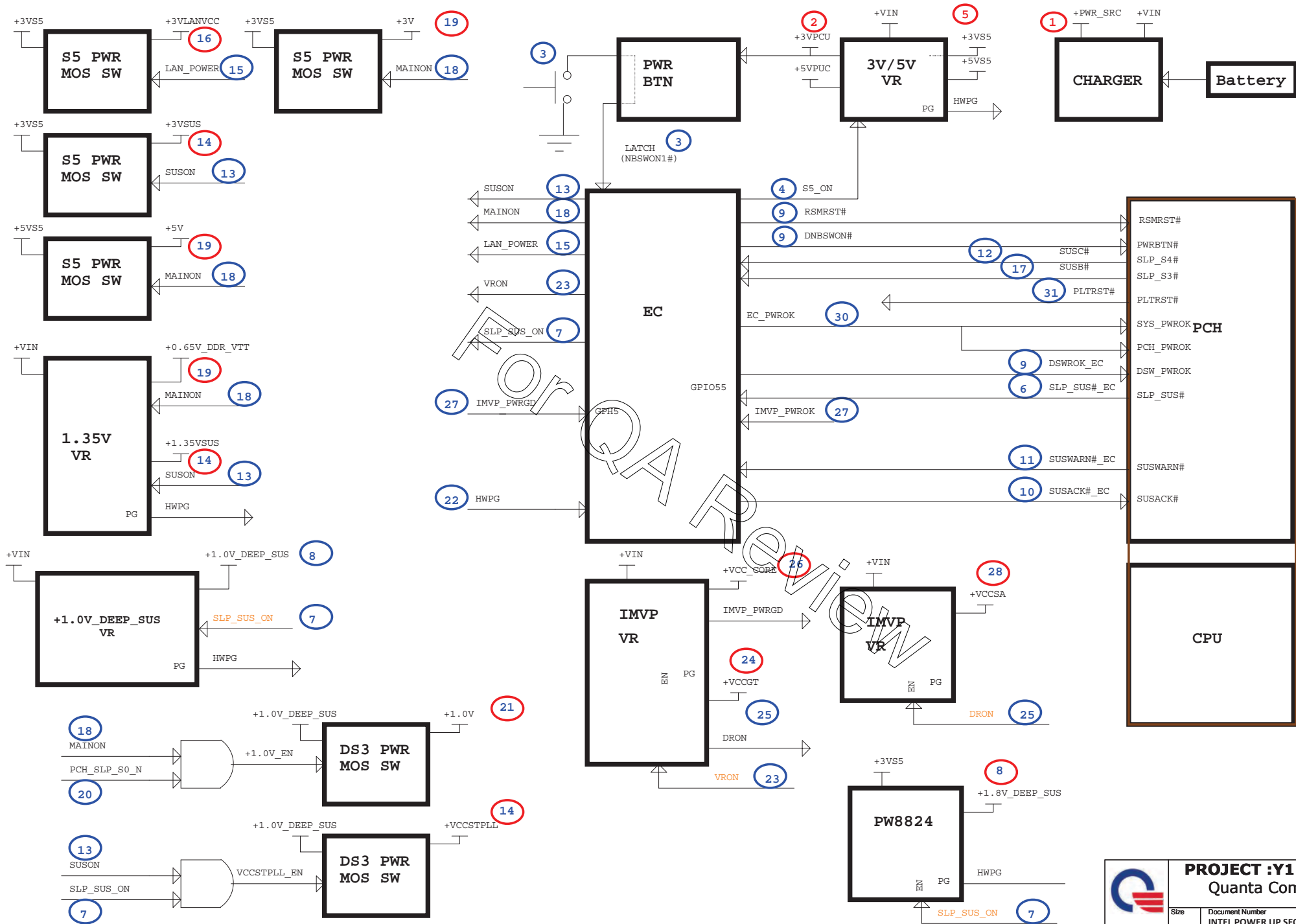
28,31,33,34,36,37,38,39,41,42,43,44,45	+VIN
4,10,15,16,32,34,35,37,39,40,43	+3VS5
4,30,32,33,37,38,39,40,41,42,43,44,45	+5VS5
3,6,17,18,38,40	+1.35VSUS
19,21,22,44	+3V_GFX
19,21,22,32	+3V_AON
19,20,21	+1.05V_GFX



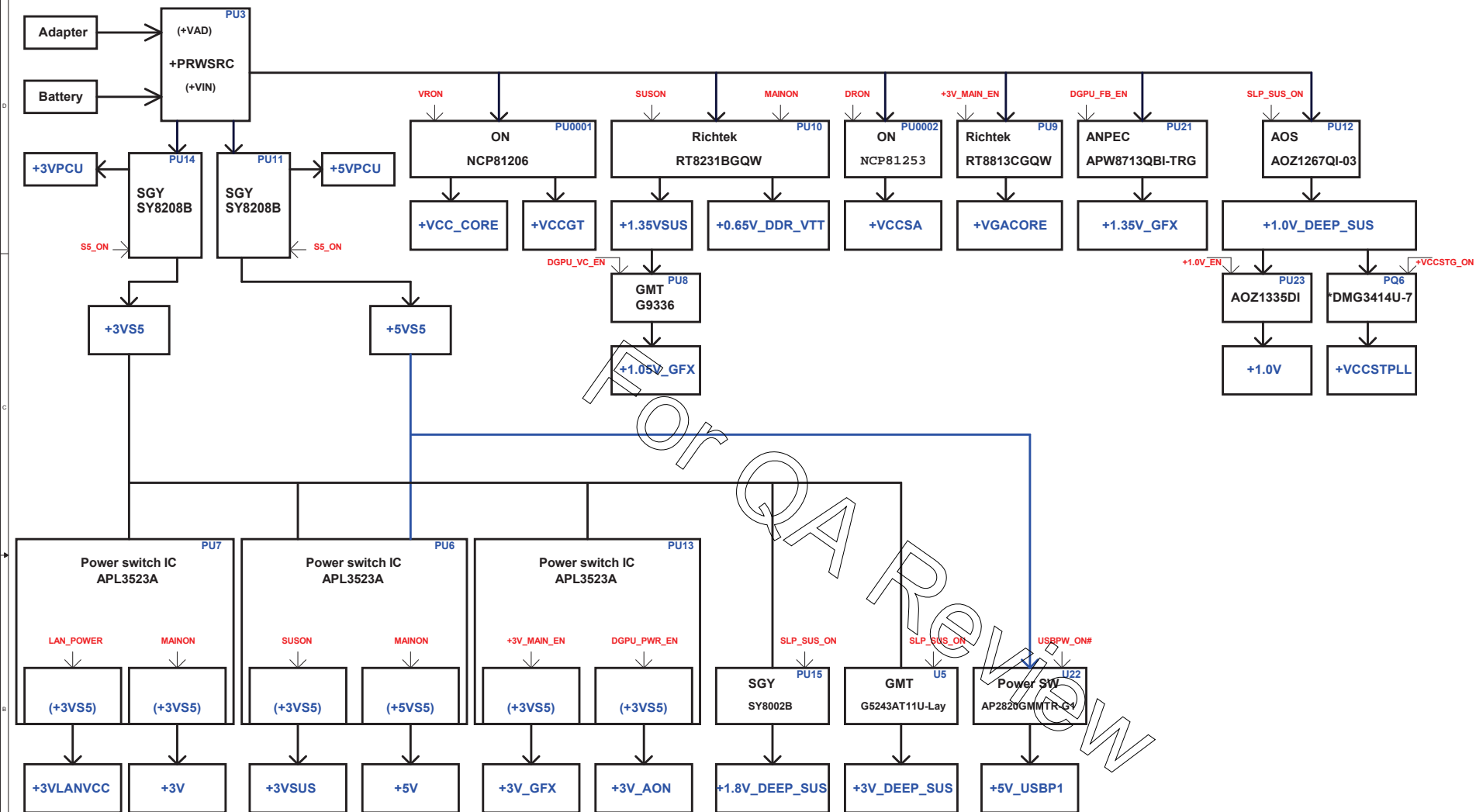
+1.05V\_GFX +/- 5%  
Continue current: 0.79A  
Peak current: 2.09A

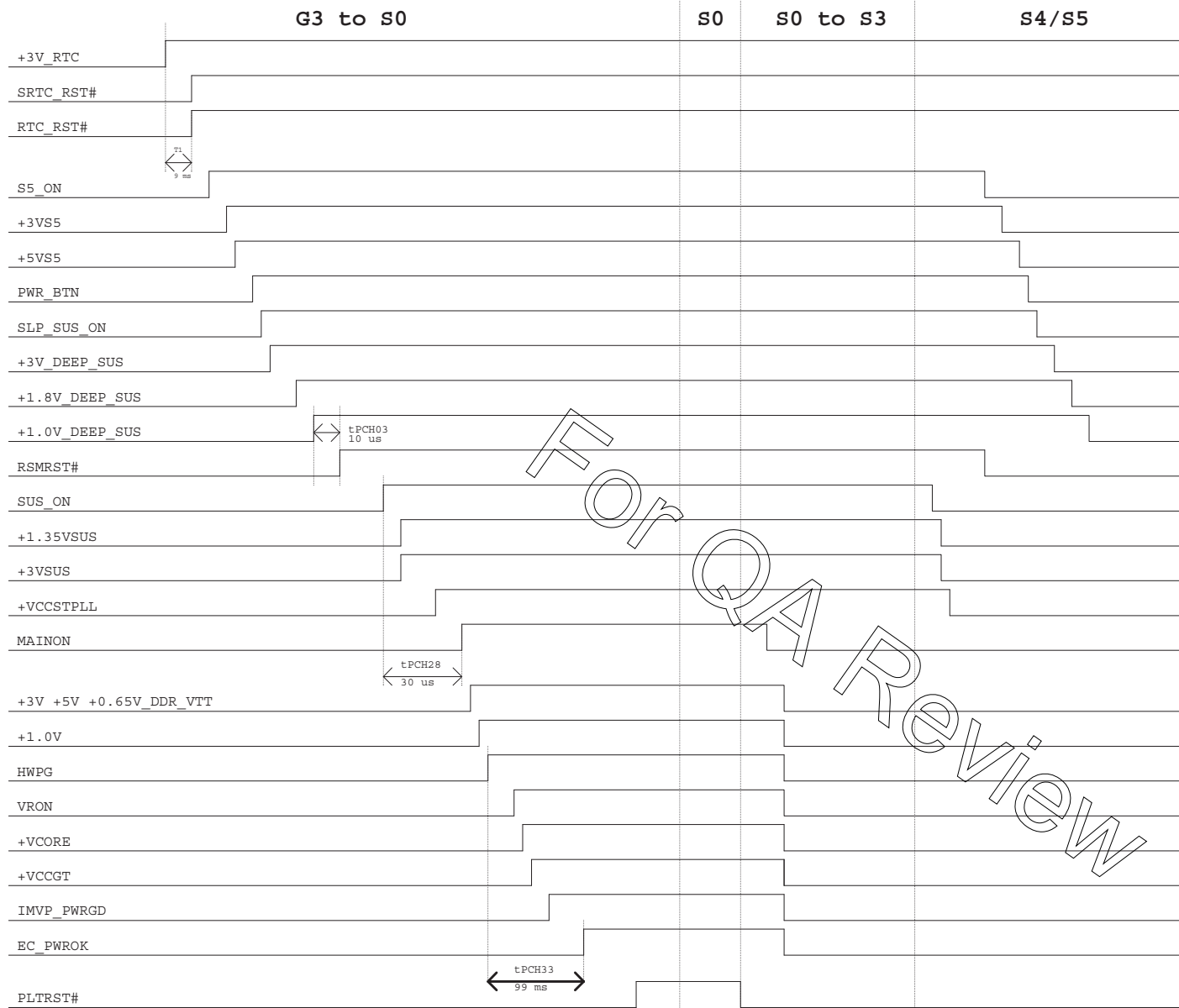


		<b>PROJECT :Y11X-6L</b> Quanta Computer Inc.	
Size Custom	Document Number 3V_GFX/1.05V_GFX[APL3523]	Rev 1A	
Date: Wednesday, May 06, 2015	Sheet	46 of	49









**PROJECT :Y11X-6L**  
Quanta Computer Inc.

Size	Document Number	Rev
	Intel POWER UP SEQUENCE	1A
Date:	Wednesday, May 06, 2015	Sheet 49 of 49